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ADVANCED ON-BOARD SIGNAL PROCESSOR GALLIUM ARSENIDE MEMORY

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This report covers the second two quarters of the AOSP Memory Program. The program is focused on the development of a low power GaAs static memory technology capable of 4K bit complexity levels. During this reporting period work continued on RAM arrays using two mask sets; the first mask set (AP1) was used for preliminary RAM cell design analysis as well as for verification of layout rules. The second mask set (RM2), using the data from AP1, focused on the design, fabrication, and evaluation of 256 bit

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RAMS. Processing techniques for incorporation of megohm CERMET resistors, and control of the required lower voltage were successfully demonstrated Testing of single RAM cells, both with external and on-chip resistors, verified cell operation, established operating windows, and demonstrated the effects of resistor non-uniformities. Preliminary yield analysis for the first four wafers(224 bit undecoded arrays) showed a failure rate of ≈ 1% and a circuit yield of ≈10%.

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TECHNICAL SUMMARY

This report covers the second six months of the AOSP Memory Program. The objective of this program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of a 4K bit RAM. The DARPA process development program has complemented and provided a sound basis for the initial progress made in this RAM program. Using the existing GaAs technology as a base we have initially focused our efforts on process areas unique to RAMS, on evaluation of the power concentration RAM cell and on the design of a 256 bit static memory chip.

The development of operational 256 bit memory arrays has been based on two mask sets; namely AP1 and RM2. Mask set AP1 contained preliminary RAM cell designs for verification of design concepts and layout rules while RM2, using the data obtained from AP1, focused on the design, fabrication and evaluation of 256 bit RAMs.

Preliminary Mask Set AP1

The first mask set, AP1, was used as a test vehicle for the evaluation of design rules, measurement of device and substrate characteristics, development of megohm resistors, and performance mapping of individual RAM cells and simple arrays. The device test results obtained from this mask set revealed a number of parameters directly applicable to the design and operation of 256 bit arrays. These parameters include: (1) acceptable leakage currents of < 1 nA at normal FET operation voltages, (2) a forward voltage drop of 0.45 V for level shifting diodes, and (3) reliable operation of low threshold (V_p = 0.5 V) FETs in the 10-100 nA range. In addition, a fabrication technique for cermet ($Cr:SiO_x$) megohm resistors was developed and incorporated into several of the AP1 wafers. In this way cell operation using both on-chip cermet resistors as well as external resistors, could be evaluated and compared. The bistable operation range for the individual RAM cells was

determined as a function of power supply voltage, and effects of resistor non-uniformity were measured. Analysis of megohm cermet resistor test results indicated that this approach is a viable technology for the 4K RAM. Finally, preliminary yield data from this mask set indicated that tightened design rules with 2, and 4 μm FETs was a viable option (from a processing standpoint) for future RAM cell designs.

RAM (256 bit) Array Design (RM2 Mask Set)

Using the AP1 test results as a guide, the second mask set, RM2,was designed. In addition to the cell arrays, a preliminary design was also made for the decoder circuits. Three 256 bit arrays (with decoders) were included: these were (1) the baseline low power cells, (2) a high power version with four times the current level, and (3) a low current version with three diodes instead of two. Another array with 224 baseline cells without decoders was also included for direct probing.

RAM Process Development

Processing of the RM2 (256 bit RAM) wafers proceeded using normal planar GaAs fabrication methods except for two process areas which are characteristic of the low power requirements of RAM arrays; namely, control of a lower threshold voltage (0.5 V) FETs and incorporation of an additional mask level for the megohm cermet resistors. These two exceptions to the standard IC process presented minimal problems for wafer fabrication. Measurements of threshold voltages showed a standard deviation over the wafers of less than 100 mV (with typical values in the 60 mV range), while resistor values showed a uniformity of better than ± 10%. In addition, the process monitor values such as diode series resistance and ohmic contact resistance were all within normal bounds for the wafers tested.

RM2 Performance Results and Yield

Testing of the undecoded arrays on RM2 was done using an automated probe station and test microcomputer system. Each cell in the array was tested and a map of the array was produced showing the location and type of failure encountered, e.g., failure to write "1" or "0". These failure maps are being used as an aid, first, in visual inspection of failed cells to determine obvious failure causes, and then for subsequent, more thorough electrical testing. Data from this testing will be used to establish the yield model that will guide process, layout, and design improvements that will be needed to attain the yield level required for producibility of 4K RAMs.

The measurements made on the undecoded 224 bit arrays provide preliminary statistics on yield of the RM2 low power cell design. Four wafers were tested, each with 36 arrays of 224 bits per array. Thus, 32,256 cells were available for test. Of the arrays, 3 had power supply shorts, and, thus, could not be tested. Therefore, 33 arrays (31,584 cells) were tested. There were 14 perfect arrays, distributed 3, 3, 5, and 3 per wafer. The yield of perfect arrays was $14/(4 \times 36) = 10\%$. This yield, for essentially a first design, is an adequate starting point for leading to a 4K RAM development.

1.0 INTRODUCTION

The objective of Phase I of the GaAs RAM program is to utilize the performance advantages offered by GaAs integrated circuits in the areas of radiation hardness, low power dissipation and high speed for the development of 256 bit RAM. Under our DARPA process development program, great strides have been made toward successful development of an ion implanted planar GaAs LSI/VLSI compatible processing technology. This GaAs technology development program has ideally complemented and provided a sound basis for the initial RAM development. The technology development strategy used in this program, therefore, extends the existing GaAs technology base process in areas unique to RAMS, utilizes a power concentration RAM cell approach, and integrates both advanced design and processing concepts into a viable GaAs LSI/VLSI RAM technology.

During the past six months considerable progress has been made toward demonstrating a functional 256 bit RAM array. Two mask sets were used in this development; mask AP1 was a fast turnaround mask set that provided initial data for the design of the second mask set, RM2. This latter mask set contained the actual 256 bit RAM arrays. The RAM process development is discussed in Section 2.0 of this report where the evaluation and control of low threshold voltage is presented for both the AP1 and RM2 wafers. The progress made in the development of cermet resisters is also discussed in this section. In Section 3.0, the RAM cell and analysis for the AP1 mask set is presented. Measurement of substrate leakage, diode characteristics, and subthreshold FET conduction, along with the operating characteristics of individual RAM cells are presented. The progress made with the RM2 mask set is presented in Section 4.0 and includes the design of the 256 bit arrays, as well as testing and yield analysis undecoded 224 bit arrays. Finally, some initial radiation test results are presented in Section 5.0 which demonstrate the radiation hardness advantage of GaAs.

2.0 RAM PROCESS DEVELOPMENT

Two mask sets have been used for the development of the 256 bit RAM array, namely, mask sets AP1 and RM2. The first mask set (AP1) was used as the design and test vehicle for the future 256 bit array, and contained resistor test patterns, discrete FETs and diodes, a large matrix of RAM circuit designs, and small RAM arrays with and without on-chip resistors. Mask set RM2 contained the 256 bit RAM arrays, with and without decoding circuits, as well as resistor test patterns and individual RAM cells. The design analysis, layout considerations, and test results for these mask sets will be discussed in detail in Sections 3.0 and 4.0 The key process development issues, specifically, control of threshold voltage and fabrication of MΩ cermet resistors, will be discussed in the following section along with a summary of the process monitor results for the RM wafer lots.

2.1 Process Characterization Results (AP1)

The magnitude of the threshold voltage is one of the most difficult parameters to control because of variations in the shallow, lightly doped n^- layer. The control of this parameter is dependent not only on the reproducibility and uniformity of the processes which were used, but also on the quality of the GaAs substrates. Typically, the long range distribution of the FETs from a full GaAs IC wafer are characterized by the threshold voltage of 1.1 V with a standard deviation of 100 mV. Because the RAM cell was designed for subthreshold current operation, threshold voltages of approximately 0.5 V were required. Using the AP1 mask set, implants were systematically varied in order to evaluate proper dose and substrate conditions necessary for $V_p = 0.5$ V. For a dose of 2.2×10^{12} cm^2 at an energy of 390 keV, the resultant threshold voltage was found to be in the range of 0.85 to 0.95 V, while decreasing the dose to 2.0×10^{12} cm^2 resulted in a threshold voltage in the range of 0.50 to 0.60 V. Thus, the implant conditions of 2.0×10^{12} cm^2 at 390 keV was set as an upper limit for the processing of RM 2 wafers with reasonable assurance that the proper threshold voltage could be obtained.

After the implantation adjustments, processing of the three AP1 wafer lots continued in a normal fashion. Approximately half the wafers were fabricated without cermet load resistors so that the external resistors could be used to analyze circuit performance. The remaining wafers were processed with cermet films in order to verify resistor processing techniques which would be used on the RM2 wafer lots.

2.2 Process Characterization Results (RM2)

To date, five RM2 wafer lots (four wafers per lot) have been started, of which three lots have been carried through to completion. The process yield on these wafers has been good; one wafer (RM2-13) was rejected because of nitride lifting, one wafer (RM2-41) was misoriented, while a third wafer (RM2-42) was broken. Of the wafers that have been completed, no particular processing difficulties were encountered even though an additional mask level for resistor fabrication was added to the normal processing. The lithography, etching and metallization steps all progressed in normal fashion.

Of particular importance to the RAM development are certain process monitor parameters which are indicative of how well the process is proceeding at the various stages of fabrication. Table 2.2-1 summarizes device parameters obtained for each RAM lot using processing routines successfully adapted for the RAM fabrication. The threshold voltages of FETs are all within an acceptable range, indicative of good process control. A more detailed description of the pinch-off voltage status will be discussed in a later paragraph. In the case of the logic diodes, the series resistance, R_S, and the threshold voltage, V_{TH} have been monitored and again show acceptable values for all wafer lots. Finally, the ohmic contact measurements show that specific contact resistance, r_C, and the sheet resistivity, R_S, are all generally within normal values.

Table 2.2-1

Process Monitor Parameters for RM2 Wafer Lots - Numbers Shown are Average Value Per Lot

	FETs		Diodes		Ohmic Contacts	
Wafer Lot	V_p (V)	I_{DSS} (mA)	R_S (Ω)	V_{TH} (V)	r_c (Ω-cm^2)	R_S (Ω/□)
1	0.496	0.83	630	0.877	2.8×10^{-6}	417
2	0.518	1.12	627	0.818	3.2×10^{-6}	408
3	0.416	0.86	618	0.874	1.3×10^{-5}	315
4	0.510	1.18	632	0.859	2.3×10^{-6}	349
5	0.582	1.27	420	0.822	1.5×10^{-5}	333

Table 2.2-2 lists the resultant pinch-off data for the RM2 wafers processed to date. As can be seen the threshold voltage is generally below 0.6 V with only one wafer having a standard deviation greater than 100 mV. Thus, control of V_p as the array is extended to 4K does not appear to present a serious problem, however, the exact nature of threshold voltage variations with respect to RAM cell operation will continue to be investigated.

Table 2.2-2

Control of Threshold Voltage for RM2 Wafers

Wafer	V_p (V)	σ_{V_p} (mV)
11	0.443	97
12	0.408	60
14	0.638	53
21	0.388	54
22	0.515	147
23	0.568	95
24	0.599	73
31	0.423	57
32	0.474	50
33	0.481	48
34	0.467	73
43	0.536	52
44	0.484	55
51	0.581	38
52	0.475	40
53	0.654	45
54	0.617	62

2.3 MΩ Resistor Development

As in the case of the pinch-off voltage evaluation, the AP1 mask set served to develop the process techniques for incorporation of the cermet resistor into the RAM cell arrays. Once the fabrication steps were known, RM2 processing was begun. The results from this series of experiments are discussed in the following two sections.

2.3.1 Cermet Resistors (AP1)

The design of the AP1 test cells and arrays called for resistor values with either ≈ 5 MΩ/□ or ≈ 20 MΩ/□ sheet resistivity. In this way operating cells could be obtained depending on which resistivity value was easier to achieve. As discussed in the last semi-annual report,[1] a number of parameters were found to affect the resistivity of the r.f. sputter deposited cermet films. These parameters include composition of the sputter target, ratio of target -to-substrate voltage, pressure of the sputtering gas, and oxygen partial pressure. For the initial attempts at resistor fabrication using the AP1 mask set, the target composition was 80:20 wt% SiO:Cr, the bias voltage was zero, and the sputtering pressure of the argon was 5 mtorr. Oxygen poisoning was found too difficult to control and was, therefore, not pursued. Films deposited under these conditions showed a sheet resistivity of 2-3 MΩ/□ when measured by the 4-point probe technique. The finished, on-chip resistors, on the other hand, showed a considerable variation in resistivity value, and not in good agreement with the 4-point probe measurements. After several attempts to fabricate resistors with consistent resistivity values, an Auger analysis of the cermet films was pursued in an effort to uncover problem areas, particularly with respect to the ceremt-to-second metal contact. Figure 2.3-1 shows the atomic fraction of the surface as a function of depth for a cermet film. The high percentage of oxygen and dielectric at the surface suggests the formation of an oxide layer after exposure of the film to air. The effect of O_2 ashing for photoresist removal can also be seen in the figure. This oxide layer would make the contacting to second level metal very difficult, and could account for the spurious results which were initially observed.

One technique to avoid this problem was to simply interchange the cermet and second-level metal process steps. Instead of metal being deposited on the cermet film, as originally proposed, cermet would be deposited on second-level metal (gold). This process is shown schematically in Figure 2.3-2. Thus, the formation of oxides on the cermet film can be avoided, and

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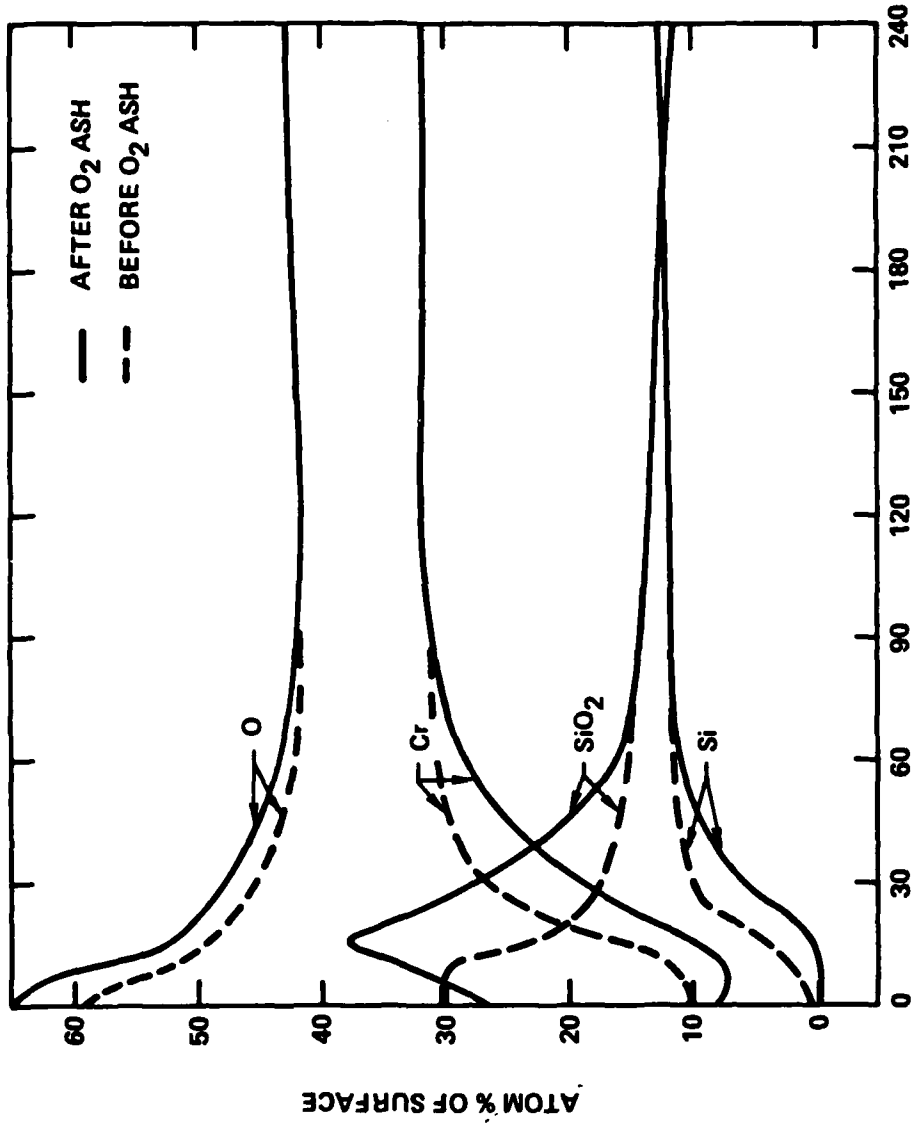
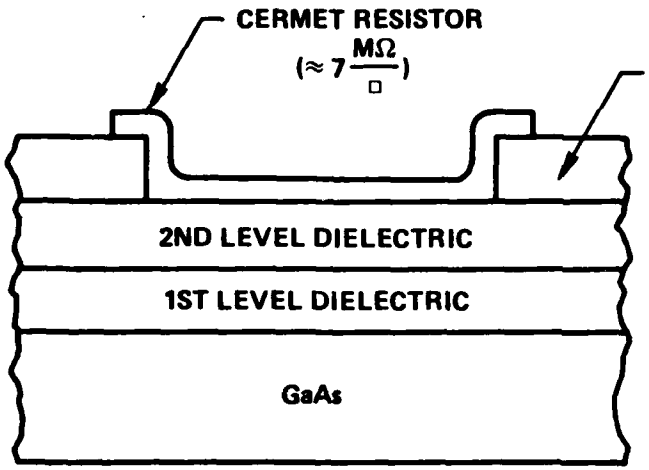


Fig. 2.3-1 Auger analysis of cermet film.



FOLLOWING 2ND LEVEL METAL

1. DEPOSIT CERMET FILM
2. MASK CERMET RESISTOR
3. ION MILL RESISTOR
4. REMOVE PHOTORESIST

Fig. 2.3-2 Cermet resistor fabrication steps.

since gold is relatively free of oxide, better contacts should result. Two wafers (AP1-31 and AP1-32) were processed in which the cermet film was deposited on both wafers at the same time. However, wafer AP1-31 had second-level metal deposited on cermet, while wafer AP1-32 had the reverse process. Measurements of sheet resistivity for the two wafers are shown in Table 2.3-1. As can be seen wafer 32 showed consistent results from the various techniques for measuring sheet resistivity, namely, a Van der Pauw "cross" pattern, a 22 □ resistor, the transmission line method, and the mechanical 4 point probe (these measurement techniques were discussed in the last semi-annual report).

Table 2.3-1

Resistor Measurements for Wafers AP1-31 and 32

Wafer	Van der Pauw (MΩ/□)	22 Resistor (MΩ/□)	TLM (MΩ/□)	2 R_C (MΩ)	4 pt. Probe (MΩ/□)
31	-	8	-	-	2-3
32	3.3	3.0	3.4	3.2	2-3

Measurement of wafer 31, on the other hand showed inconclusive results and the inability to make most of the measurements due to open test structures or scattered data. The test showed, however, that deposition of the cermet film on second metal was the preferred process and as a result would be the technique used for the RM2 mask set.

One potential problem area with the above described approach is the step coverage of the thin (≈ 3000 Å) cermet film over the thicker (4000-6000 Å) gold interconnect layer. Figure 2.3-3 shows a SEM photo of cermet resistor over a second level metal where the film thicknesses are 3000 Å 6000 Å, respectively. The step coverage is reasonably good in this case, primarily due to the slight sloping of the ion milled metal line edges. In

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Fig. 2.3-3 Step coverage of cermet on 2nd level metal.

fact, the degree of slope of the metal edge can be controlled by the ion milling techniques used, and thus, offers some additional control if necessary. Ideally, the thinner cermet film should be covered by the thicker second level metal, but additional process development will be necessary to protect the cermet film from oxidizing during subsequent processing steps. One approach would be to deposit a thin gold layer on the cermet film using the same vacuum system in which the cermet was deposited. A slight overetching of the second level metal would then clear this layer. This technique will be attempted in the future when new sputtering equipment becomes available.

2.3.2 Cermet Resistors (RM2)

The sheet resistivity value for the resistors fabricated with the RM2 (256 bit) mask set was chosen as a function of final resistor size and ease in which reproducible films could be deposited. A sheet resistivity of approximately 7 MΩ/□ was chosen as the design goal, and thus, dictated resistor sizes of 2 × 12 μm (6□) and 2 × 5 μm (2.5□). This increase in resistivity value above that of the AP1 wafers was achieved by increasing the argon sputtering pressure from 5 to 6 mtorr and by operating with a substrate bias ratio of ≈ 3%. Processing of the resistors for all the RM2 wafers was done in a manner identical to that of wafer AP1-32 in which the cermet film as deposited on second level metal. The RM2 mask set has test patterns similar to those on second level metal. The RM2 mask set has test patterns similar to those on the AP1 mask set for measuring sheet resistivity, resistor uniformity, and contact resistance. Figure 2.3-4 shows one of these test patterns as well as the completed resistors in a typical 256 bit RAM cell array. Table 2.3-1 shows the test data obtained for the three RM2 wafer lots (11 wafers) processed to date. The resistor values on the wafers were purposely kept below the design values of 50 MΩ and 22 MΩ so that ion mill thinning could be used later to optimize the resistor values. The uniformity of the resistor values over the wafer also shown in Table 2.3-1. The measurements indicate that reasonably good results can be obtained using the present fabrication

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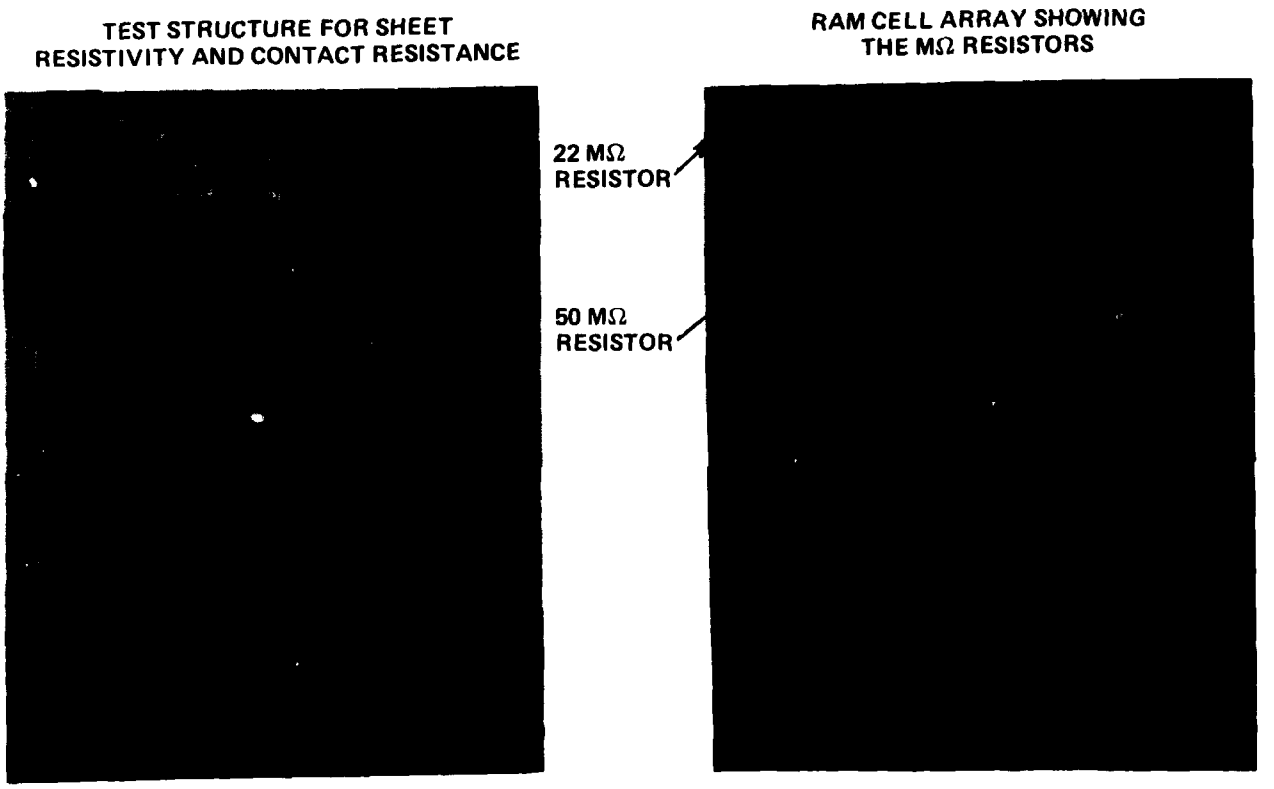

Fig. 2.3-4 Test structure and cell array for cermet resistors.

techniques, and the extension to a 4K RAM design should present no major fabrication difficulties.

Table 2.3-1

Resistor Test Results for Lots RM2 - 1, 2, 3

Wafer	Sheet Resistivity (MΩ/□)	Resistor Values 6 □ (2 × 12 μm) (MΩ)	Resistor Values 2.5□ (2 × 5 μm) (MΩ)	Contact Resistance $2R_C$ (MΩ)
11	5.5	39.9 ± 7.8%	18.9 ± 7.8%	4.2
12	6.5	44.7 ± 6.2%	20.6 ± 7.8%	3.9
14	5.7	41.3 ± 8.6%	19.6 ± 8.1%	4.7
21	6.4	38.9 ± 7.0%	17.7 ± 6.9%	3.1
22	5.7	35.3 ± 3.7%	16.3 ± 3.2%	2.4
23	6.5	39.0 ± 4.0%	17.7 ± 6.4%	2.7
24	7.3	44.2 ± 14.5%	20.5 ± 14.4%	4.1
31	6.9	43.5 ± 7.9%	20.0 ± 8.2%	3.3
32	7.5	46.2 ± 5.8%	21.8 ± 6.9%	4.1
33	7.1	47.7 ± 7.0%	22.1 ± 7.5%	3.3
34	7.3	50.3 ± 7.8%	23.6 ± 8.5%	4.3

3.0 RAM CELL DESIGN AND ANALYSIS

The most significant task in the development of a RAM technology, from a circuit design standpoint, is the design of the RAM cell itself, with low power and high yield requirements. Therefore the circuit design and test efforts have focussed on a thorough analysis of the operation of the RAM cell. The following is a discussion of the most important aspects of this work.

3.1 Device and Layout Considerations

The RAM cell that was originally proposed was throughly evaluated at the start of this program; it was later determined that two minor changes would improve switching speed.

These changes were incorporated into the RAM cell circuit shown in Fig. 3.1-1. In addition, further analysis raised questions about the performance characteristics of GaAs devices that could only be answered by fabricating and measuring various test devices and circuits. Therefore, a first mask set (AP1) that contained test devices, as well as several versions of the RAM cell in Fig. 3.1-1, was designed. Quantitative data obtained from the various test structures and cell designs contained on this mask will provide the information needed for designing 256 bit and larger RAMs.

The two most critical device characteristics for this cell design are the FET operating characteristics below pinch-off (subthreshold region) and the forward voltage drop of diodes carrying very low currents. To achieve the ~ 1 μw power level in a cell, operating currents must be in the tens of nanoamperes range, requiring verification that subthreshold currents and/or leakage currents are below this level. The voltage drop of a diode depends on current density, which can be kept high for a given current by making the diodes smaller; however, practical photolithography limits the diode to 1 μm × 1 μm. Even at this size, the operating current density is 4 orders of magnitude less than the operating current density in diodes contained in more

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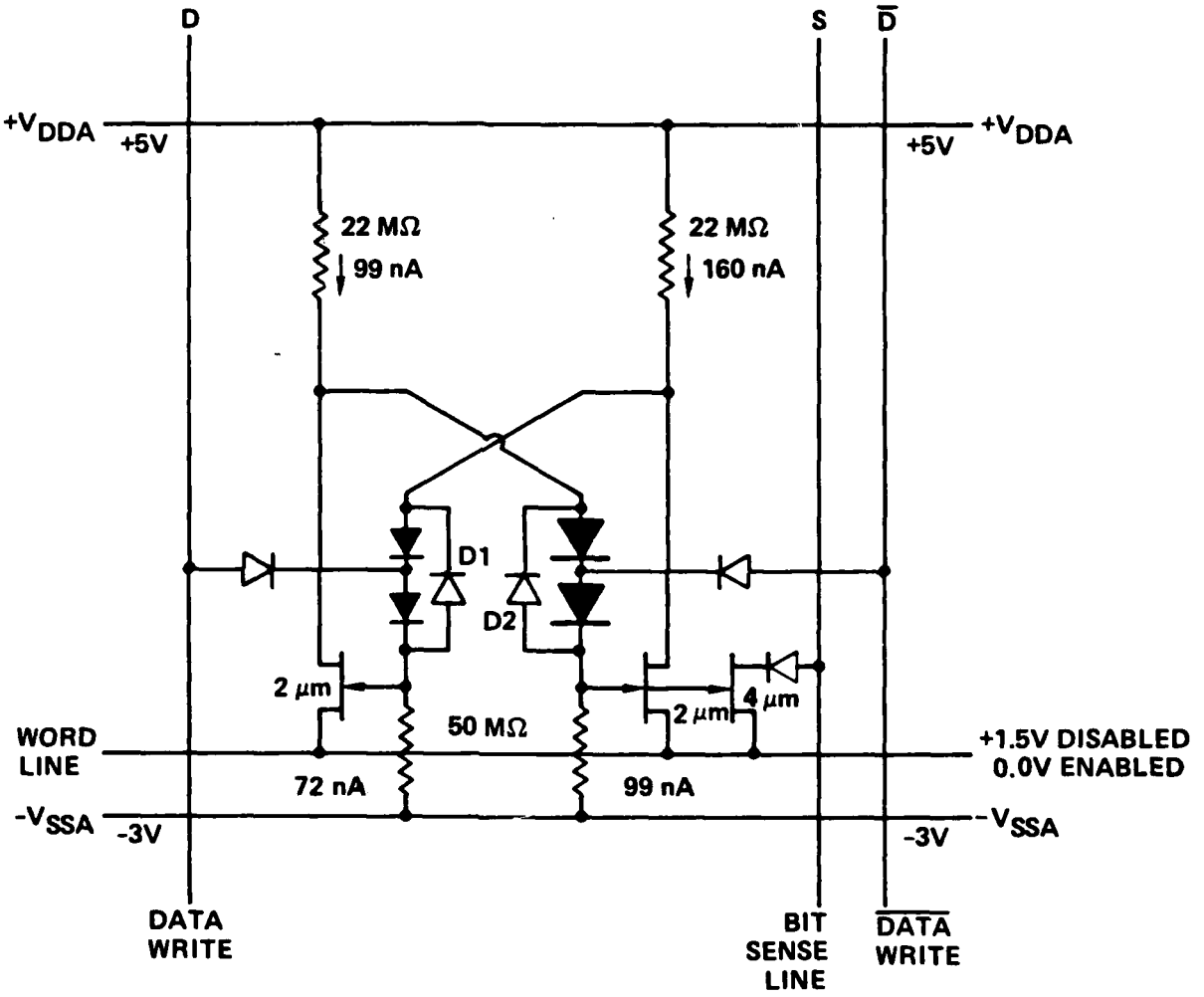


POWER/BIT = (+5) (259) + (-3) (-171) = 1.81 μW/BIT
MEMORY ARRAY STATIC POWER = 4096 x 1.81 x 10^{-6} = 7.4 mW/14K CHIP

Fig. 3.1-1 Cell for 256 bit GaAs static RAM.

conventional SDFL circuits. Verification that leakage currents are not of the same order of magnitude as the anticipated low operating current densities was needed.

At the start of this program, cermet (megohm) resistors were an untried technology, and mask patterns were needed both to develop the process, and to verify resistor performance. Also various approaches for implementing the resistor technology as well as alternative, device means for providing high impedance, low current sources should be evaluated.

The conservative layout design rules that have been established for the general Rockwell GaAs IC process are not necessarily consistent with all types of circuits. These design rules have been followed to the letter in the MRDC MSI/LSI circuits in which internal (gate circuit) yield is critical to achieving test parts. However, these design rules may be altered with judicious care for sake of increased speed and/or density. For the proposed 4K RAM, the cell size should be kept to an absolute minimum both to minimize power (by keeping line capacitances low, in part), and to keep the overall chip dimensions (with their attendant adverse affect on chip yield) as small as possible. The specific design rule limitations must be determined experimentally. A practical balance between performance and yield must be achieved through careful analysis of experimental device and circuit results. These considerations were addressed in the design of the first RAM mask set.

3.2 First RAM Mask Set (AP-1)

The purpose of the first mask set (AP-1 from AOSP-1) was to permit the issues discussed above to be resolved well enough that a reasonable cell design could be made for a 256 bit array. To the maximum extent possible, this mask was to include structures to answer or verify all parameter questions anticipated that would affect the final design of a RAM cell. It contained resistor patterns, individual devices in various sizes, and arrays of cell design variations. It also contained three 32 bit arrays to be used

for preliminary yield information. These three arrays consisted of the two "best" cell design choices and a control version with a cell using standard design rules.

The variables in the RAM cell design are the FET size, the cermet resistor sheet resistivity, and the design rule spacing. Table 3.2-1 lists the cell design variations available on mask AP1. A range of FET sizes were included in order to determine whether a lower limit will be reached where fringe effects (rather than uniform current flow) will dominate the FET behavior. With this design, processing uniformity of the various size FETs could also be determined. High sheet resistivity (20 MΩ/□), small cermet resistors were also included in the cell matrix as well as a more readily achievable larger (5 MΩ/□) resistors. Different resistor layouts were made to achieve the design resistor values with either sheet resistivity by varying the resistor length (indicated by short or long in Table 3.2-1). Cells were also included with connections for external resistors.

An example layout for the 2, 4 μm FET cell with normal design rules and low resistivity cermet is shown in Fig. 3.2-1. The serpentine resistors dictated the cell size. This size was maintained for the other versions, to facilitate arraying the different cells. The layout for 2, 4 μm FETs with normal design rules and a high resistivity film is shown in Fig. 3.2-2. The difference in the resistors can readily be seen. The spacings of Schottky metal are 2 μm, and vias between metal layers are located away from the source or drain regions of the FETs. Figure 3.2-3 shows the same layout with tightened rules where the Schottky metal spacings are 1.5 μm, and the vias are located right on the source and drain regions. The idea behind this mask was to avoid the expenditure of extensive layout design time; therefore no attempt was made to shrink cell size when reduced spacings and smaller components were used in design variations. These cell layout variations are the critical yield and performance determining factors. Once the best design rules are determined and proven, an optimized cell layout will be designed on a later mask set.

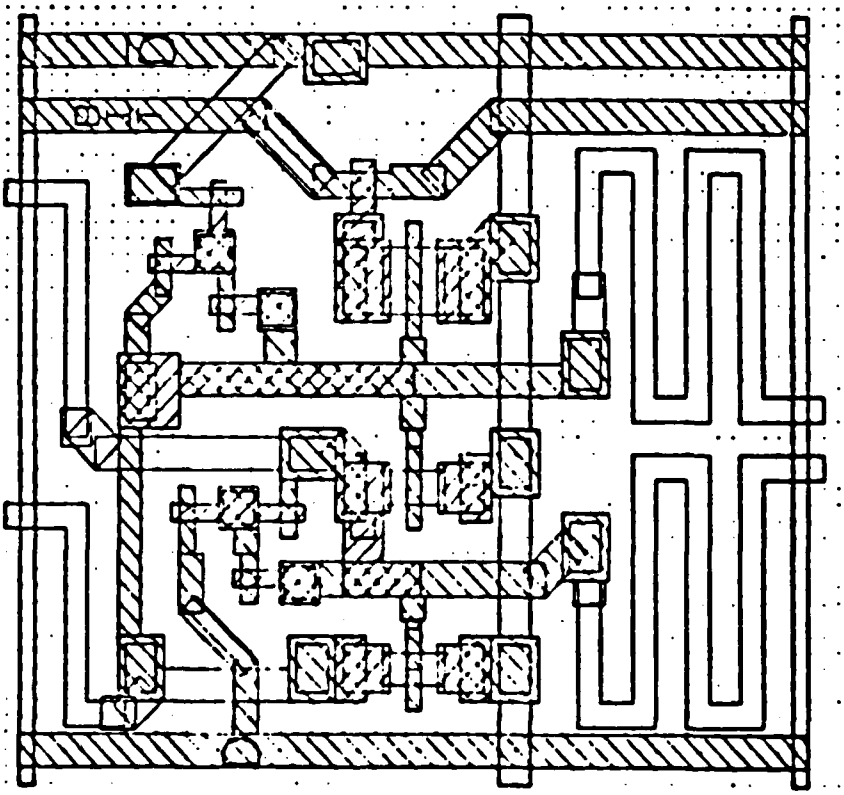


Fig. 3.2-1 RAM cell for low resistivity film, normal design rules, 2 and 4 μm FETs.

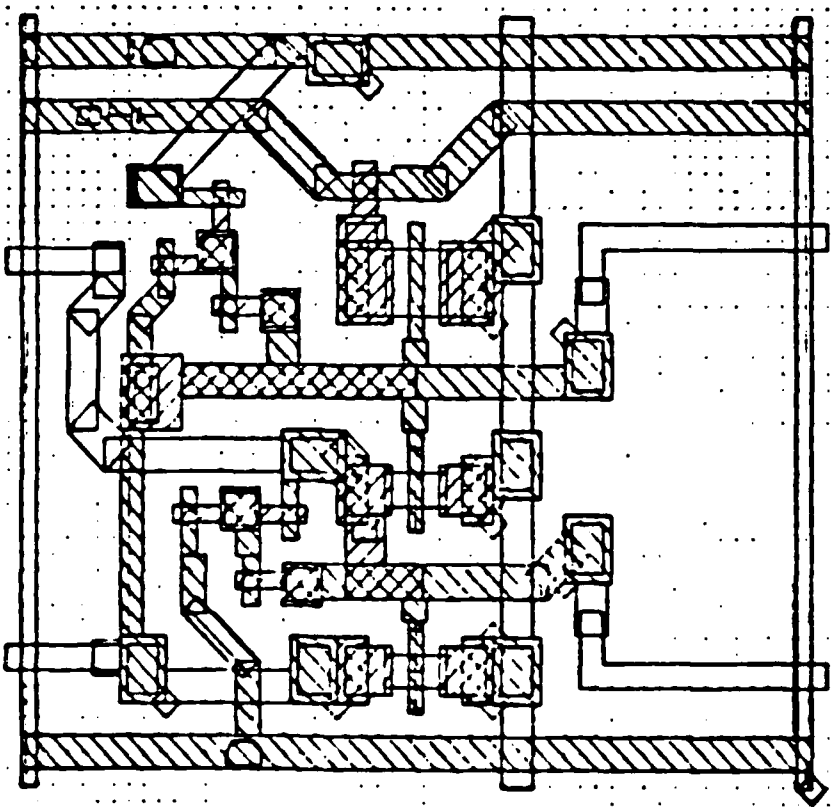


Fig. 3.2-2 RAM cell for high resistivity film, normal design rules, 2 and 4 μm FETs.

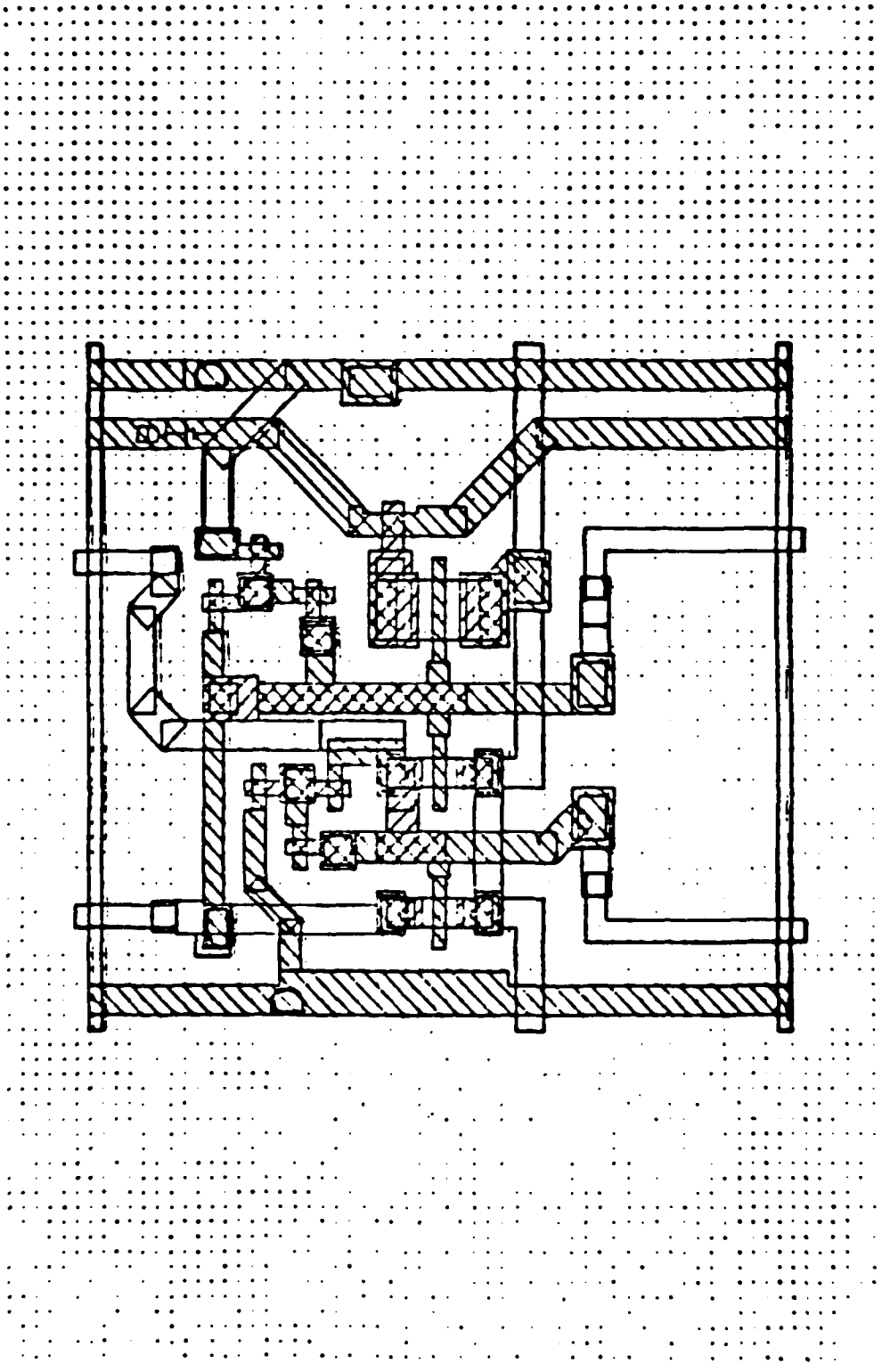


Fig. 3.2-3 RAM cell for high resistivity film, tightened design rules, 2 and 4 μm FETs.

Table 3.2.1
Design Variations of the RAM Cell

Cell	Device Sizes (μm)	Design Rules N = Normal T = Tightened	Resistors Int = Internal Ext = External	
1	1, 2	N	Int, short	
2			Int, long	
3	1, 2	N	Ext	
4	2, 4	N	Int, short	Included in RAM array A
5			Int, long	
6	2, 4	N	Ext	
7	2, 4	T	Int, short	
8			Int, long	
9	3, 6	N	Ext	
10	3, 6	N	Int, short	
11			Int, long	
12	3, 6	T	Int, short	Included in RAM array B
13			Int, long	
14	5, 10	N	Int, short	
15			Int, long	
16	5, 10	N	Ext	
17	8,15	N	Ext	Included in RAM array C

Two generic cell layouts were made, one for the cells with larger FETs (5, 10 μm and 3, 6 μm) and one for those with smaller FETs (2, 4 μm and 1, 2 μm). For each of the two, all the variations were made, and a four by eight array formed with the cell design variations scattered through it. For each size, the cell with external resistors appeared only twice; all others

appeared either four or five times, at least once in a completely internal location (for evaluation of any proximity effects). The arrangements of RAM arrays A and B are shown in Figs. 3.2-4 and -5 respectively. The quantity of a given cell variant in these arrays is sufficient for a coarse yield estimate, and good enough to identify and rule out cell designs with very low yield. The two cell designs that were considered "best", and a third very conservative control cell, were each arrayed into 4 × 8 RAMS. Tests on these arrays would provide statistical data for preliminary yield analysis.

In addition alternative current limiting circuits, consisting of a FET and one or more diodes were also included on the mask, as well as: small FETs for evaluation; diode leakage test patterns; cermet resistor patterns; patterns for alternate resistor fabrication methods; and other process monitor test cells. The organization of mask AP1 is shown in Fig. 3.2-6.

3.3 RAM Cell (AP1) Test Results

The following is a summary of the test results obtained from measurements on devices from mask set AP1. To evaluate the substrate leakage current, the IV characteristics of an isolation pattern were measured. The pattern consists of two contacts 50 μm wide with a 3 μm gap between them. Figure 3.3-1, shows the typical characteristic of the substrate leakage current, which follows a Lampert-Rose type of conduction.[2] The maximum voltages across FETs in a cell will be ~ 1.5 V. The measured leakage at this voltage, when scaled to the size of the FETs to be used in the RAM cell (2 μm) is of the order of one nanoampere, which is compatible with the design of a submicrowatt RAM cell.

Diodes are used in GaAs circuits for voltage level shifting. For appreciable current densities, the forward voltage drop across a diode is normally ≈ 0.7 V. In the RAM-compatible lower current range the voltage drop is much lower. The I-V characteristics of level shifting diodes were measured on 10 parallel 1 μm × 1 μm diodes as shown by Fig. 3.3-2. The measurement result indicates that in the current range of tens to hundreds of nanoamperes

1, 2 μm SHORT R	1, 2 μm SHORT R	2, 4 μm TIGHT RULES SHORT R	2, 4 μm SHORT R
1, 2 μm LONG R	1, 2 μm SHORT R	2, 4 μm TIGHT RULES LONG R	2, 4 μm LONG R
2, 4 μm TIGHT RULES SHORT R	1, 2 μm LONG R	2, 4 μm TIGHT RULES LONG R	2, 4 μm SHORT R
1, 2 μm EXT R	1, 2 μm LONG R	2, 4 μm LONG R	2, 4 μm EXT R
1, 2 μm EXT R	1, 2 μm LONG R	2, 4 μm LONG R	2, 4 μm EXT R
2, 4 μm TIGHT RULES SHORT R	2, 4 μm TIGHT RULES LONG R	2, 4 μm SHORT R	2, 4 μm TIGHT RULES SHORT R
2, 4 μm LONG R	1, 2 μm SHORT R	2, 4 μm LONG R	2, 4 μm TIGHT RULES LONG R
2, 4 μm SHORT R	1, 2 μm SHORT R	2, 4 μm SHORT R	2, 4 μm TIGHT RULES SHORT R

Fig. 3.2-4 RAM array A on mask set AP1.

3, 6 μm SHORT R	3, 6 μm SHORT R	3, 6 μm TIGHT RULES SHORT R	5, 10 μm SHORT R
3, 6 μm LONG R	3, 6 μm SHORT R	3, 6 μm TIGHT RULES LONG R	5, 10 μm LONG R
3, 6 μm TIGHT RULES SHORT R	3, 6 μm LONG R	3, 6 μm TIGHT RULES LONG R	5, 10 μm SHORT R
3, 6 μm EXT R	3, 6 μm LONG R	5, 10 μm LONG R	5, 10 μm EXT R
3, 6 μm EXT R	3, 6 μm LONG R	5, 10 μm LONG R	5, 10 μm EXT R
3, 6 μm TIGHT RULES SHORT R	3, 6 μm TIGHT RULES LONG R	5, 10 μm SHORT R	3, 6 μm TIGHT RULES SHORT R
5, 10 μm LONG R	3, 6 μm SHORT R	5, 10 μm LONG R	3, 6 μm TIGHT RULES LONG R
5, 10 μm SHORT R	3, 6 μm SHORT R	5, 10 μm SHORT R	3, 6 μm TIGHT RULES SHORT R

Fig. 3.2-5 RAM array B on mask set AP1.

<table>
<tr><td>T2</td><td rowspan="2">FAT
FET
(CV)</td><td rowspan="2">FULL ADDER
WITH CORNER
GATE</td><td rowspan="2">RAM
ARRAY
WITH
DAMAGED
RESISTORS</td><td>CURRENT
LIMITERS
1 μ & 2 μ</td><td>CERMET RES
1.0 μ,
DAMAGED R TEST</td></tr>
<tr><td>T1</td><td>CURRENT
LIMITERS
3 μ & 4 μ</td><td>CERMET RES
1.5 μ</td></tr>
<tr><td rowspan="2">FAT
FET
(CV)
MOM</td><td>ELECT. ALIGN.
TEST</td><td colspan="2" rowspan="2">ANALOG GAIN TEST</td><td>CURRENT
LIMITERS
5 μ & 3/4 μ</td><td>CERMET RES
2.0 μ</td></tr>
<tr><td>DYN. RAM
TEST CELL</td><td>FETS
1 μ, 3 μ, 0.75 μ</td><td>DIODE LKGE
TESTS</td></tr>
<tr><td colspan="2">RAM A
RAM CELL VARIETY
WITH SMALLER FETS</td><td colspan="2">RAM B
RAM CELL VARIETY
WITH MEDIUM FETS</td><td colspan="2">RAM C
RAM CELLS
WITH LARGE FETS;
ALSO TIGHT RULES
VERIFICATION CELLS</td></tr>
<tr><td colspan="2">RAM 5
RAM CELL ARRAY
WITH SMALLER FETS,
TIGHT RULES</td><td colspan="2">RAM 8
RAM CELL ARRAY
WITH MEDIUM FETS,
TIGHT RULES</td><td colspan="2">RAM 7
RAM CELL ARRAY
WITH MEDIUM FETS,
NORMAL RULES</td></tr>
</table>

Fig. 3.2-6 Organization of mask set AP1.

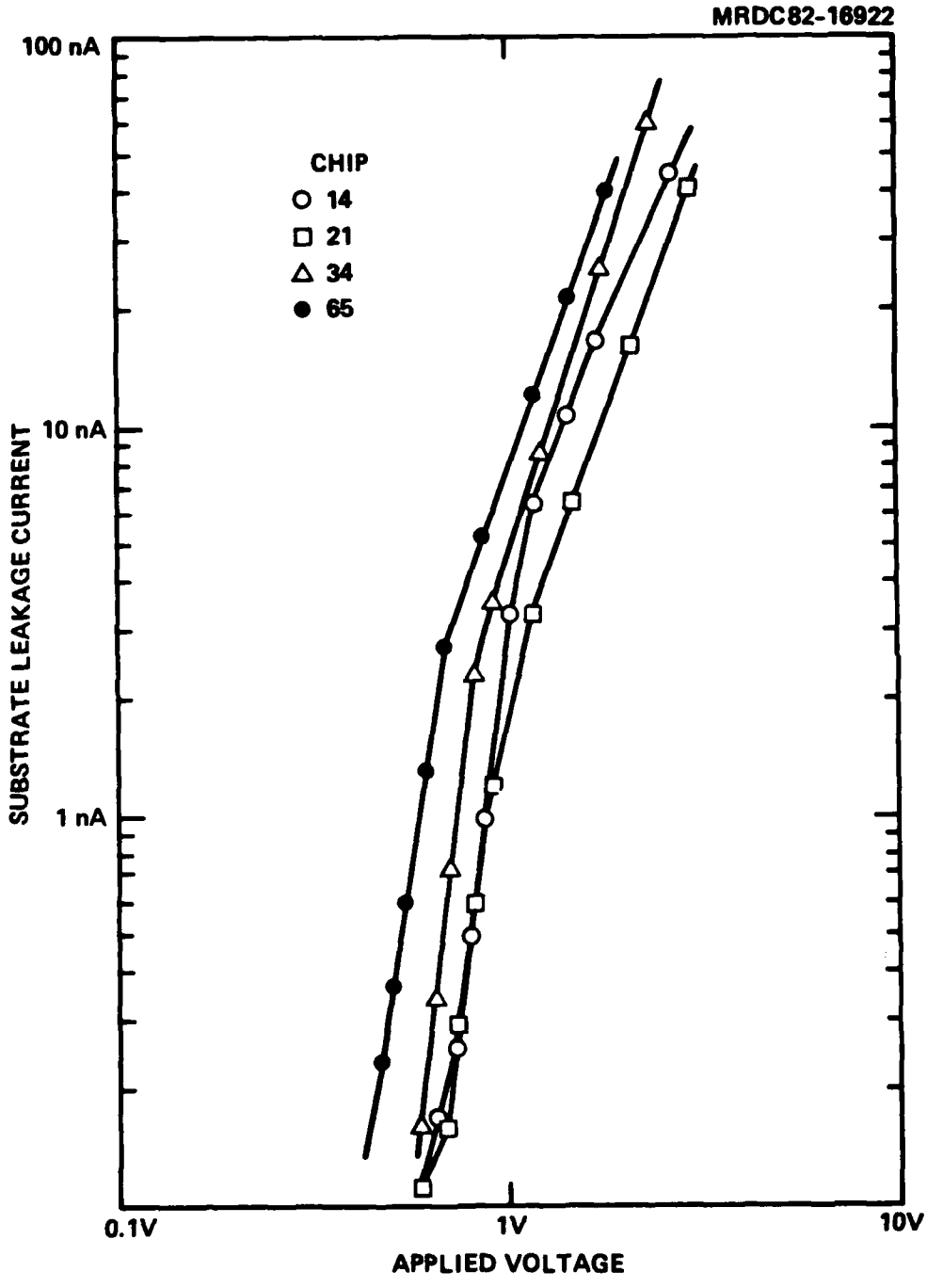


Fig. 3.3-1 Subthreshold leakage current.

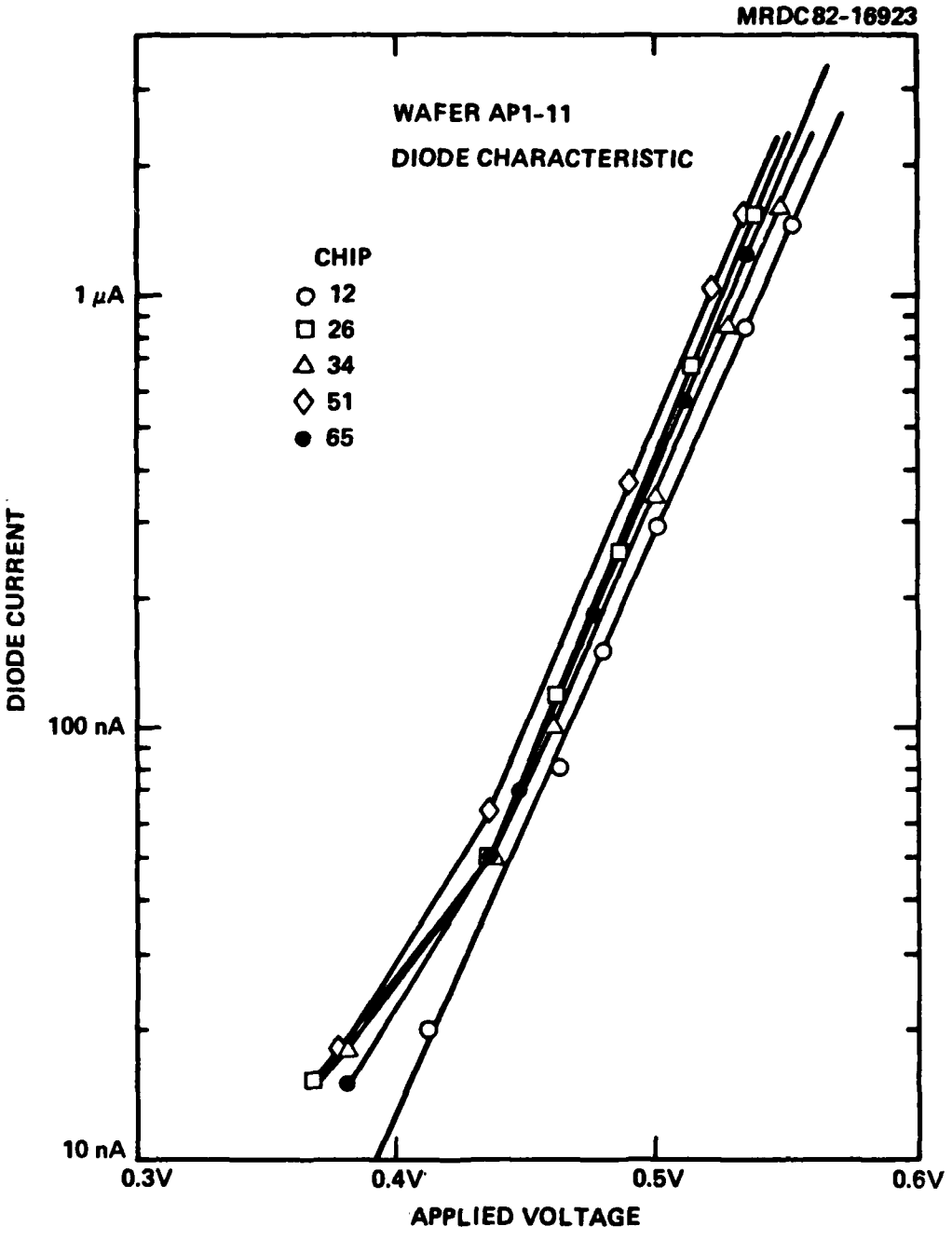


Fig. 3.3-2 Wafer AP1-11 diode characteristic.

the voltage drop across one diode ranges between 0.45 V and 0.52 V (instead of 0.7 V). In this measurement it was also found that the characteristics of doubly implanted diodes were subject to more variability and higher dark currents than were those of singly implanted diodes. Therefore, in designing the diodes for the RAM cell, singly implanted diodes will be used.

The FETs in a RAM cell are operated in the subthreshold conduction region, in which the operating characteristic departs from the square law $I = K(V_{gs}-V_T)^2$. Measurements of the low current characteristics of 2 μm switching FETs were made as shown in Fig. 3.3-3. In Fig. 3.3-3, the subthreshold conduction of these FETs can be represented as $I = I_o \exp(-\alpha q V_{gs}/kT)$, instead of square law. It can also be seen from this measurement that to decrease the current by one decade requires a change in V_{gs} of approximately 150 mV. This figure can serve as a design guide in defining the low current turnoff voltage of a FET. For example, if low current turnoff is defined as a one order of magnitude decrease in current, it can be taken as a voltage magnitude 0.15 V greater than the nominal pinch-off voltage. The measurement results shown in Fig. 3.3-1, -2 and -3 provide a preliminary set of design parameters, and verify the viability of RAM cell operation in the 10 to 100 nanoampere range, with regard to current leakage margins and device behavior.

Testing procedures for cell operation included plotting output voltage as a function of the negative supply voltage, V_{SS}, with a fixed V_{DD} and word line voltage ($V_{word\ line}$). When V_{SS} is increased negatively, from 0, with $V_{word\ line} = 0$, the curves of Fig. 3.3-4 result. With V_{SS} near 0 V, both latch FETs and the output FET are on, the voltages at the drains of the latch FETs are 0 V, and the output voltage is one diode drop above ground (≈ 0.6 V). As the magnitude of V_{SS} is increased the gates of the transistors become negatively biased, current flow is limited, and the output voltage rises. The situation is that of a balanced amplifier. Further increases in V_{SS} bring the gate voltage to $V_{pinch\text{-}off}$, at which point the circuit becomes bistable; the output will be high or low depending on the state of the latch circuit. $|V_{SS}|$ can now be increased over a considerable range with bistable operation

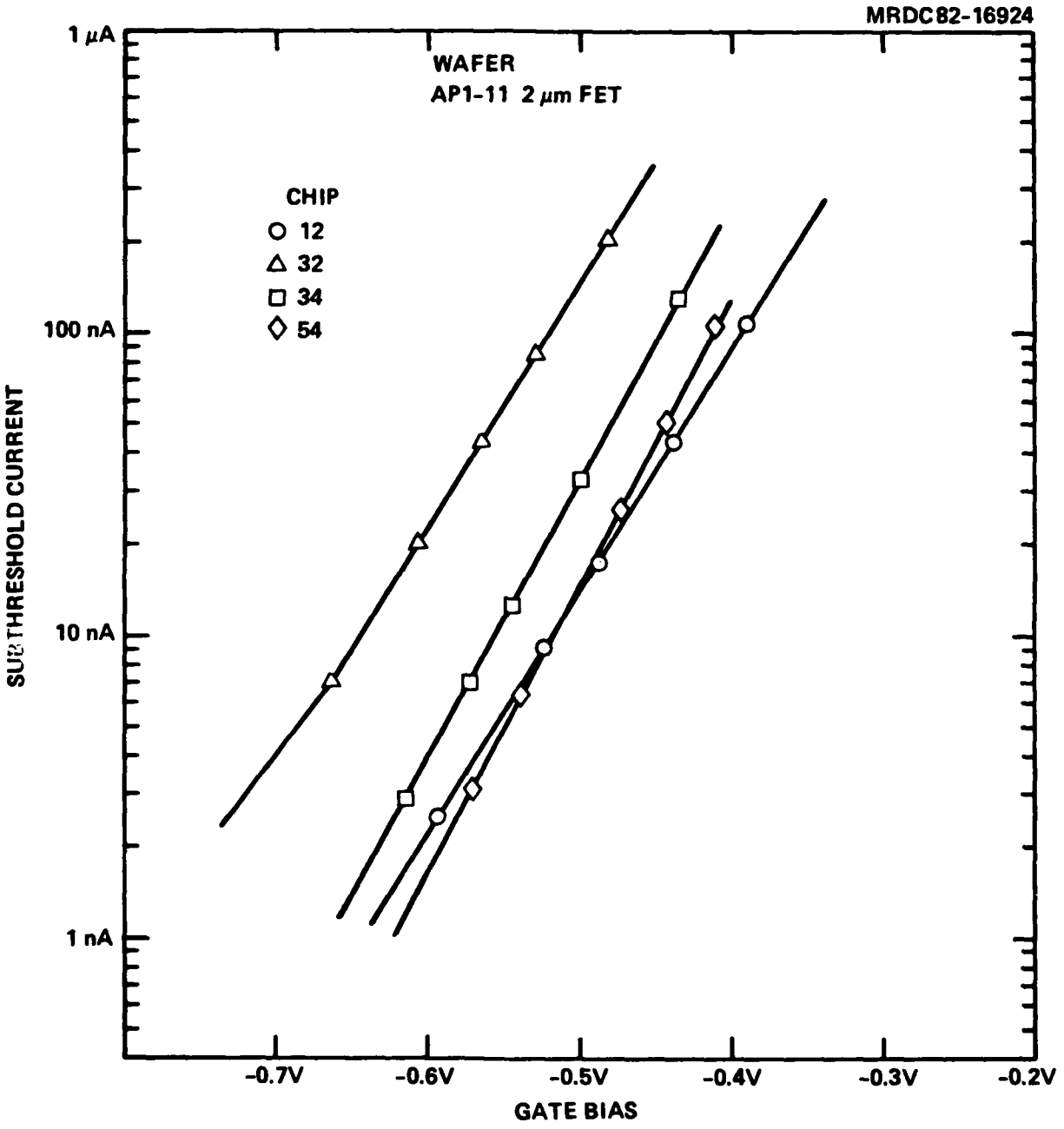


Fig. 3.3-3 Subthreshold conduction of FET.

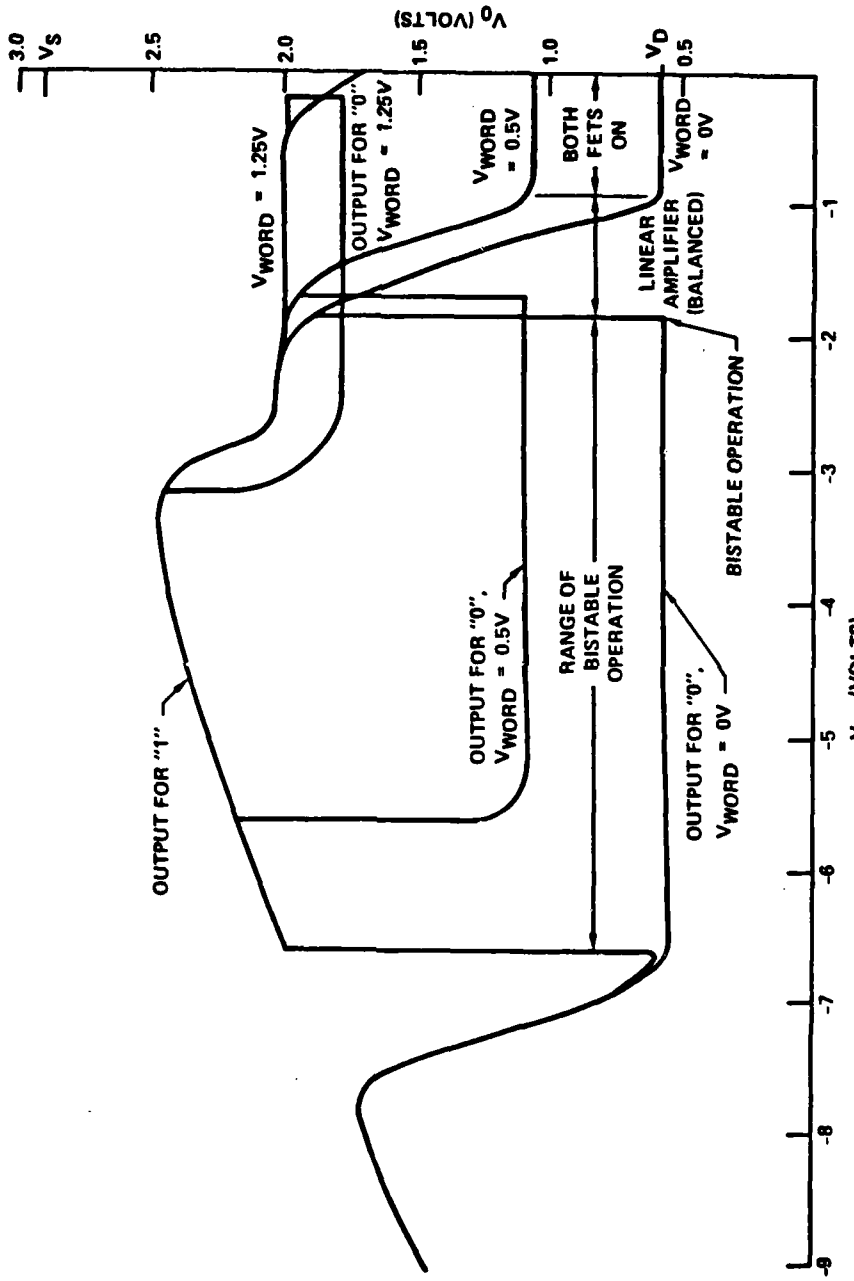


Fig. 3.3-4 Operation region for RAM cell.

maintained. Eventually it becomes so negative that the "on" FET has its current reduced to where it will not clamp the drain voltage to 0 V, which starts to rise. Near this point, the circuit loses its bistability as the voltage on the drain of the "on" FET rises and no longer holds the gate of the "off" FET below pinch-off. This gives the margin of operation for V_{SS} with a given V_{DD}, and with $V_{word\ line} = 0$; the margin is wider for higher values of V_{DD}.

The disabling characteristic of the cell can be determined by repeating the test described above, with $V_{word\ line}$ set at various voltages as shown in Fig. 3.3-5. As $V_{word\ line}$ approaches the full disabling voltage of 1.5 V, the distinction apparent in the output betweeen a "1" and a "0" disappears, and the range of V_{SS} for bistability decreases. The curves in Fig. 3.3-5 are measured data for a specific circuit with 2 and 4 μm FETs and tight design rules.

The effect of V_{DD} variations on the operating window are shown in Fig. 3.3-6. In this measurement, a very high value of sense voltage on the output was used; any output voltage above approximately 2.0 V is to be regarded as a "1", and the remaining structure of the figure (above 2.0 V) to be ignored, since in an array the output voltage would be clamped. The predominant effect of 0.5 V change in V_{DD} is to produce an approximate 1.0 V widening of the operating region for a stored "0" (the lower part of the loop) with respect to V_{SS}; the widening takes place in the high V_{SS} end, with almost no change in the low V_{SS} end. From these data it can be concluded that the cell is not particularly sensitive to V_{DD} variations.

The effect of resistor variation on the cell operating window was also verified experimentally. For a cell with external resistors, the values were set at nominal, and the operating window plotted as shown in Fig. 3.3-7. Then, in turn, the pullup resistor was increased by 10%, the pulldown resistor was increased by 10%, and finally both resistors were increased by 10%. As would be expected, since the circuit operation depends on the ratio of the resistors more than absolute value, increasing both had

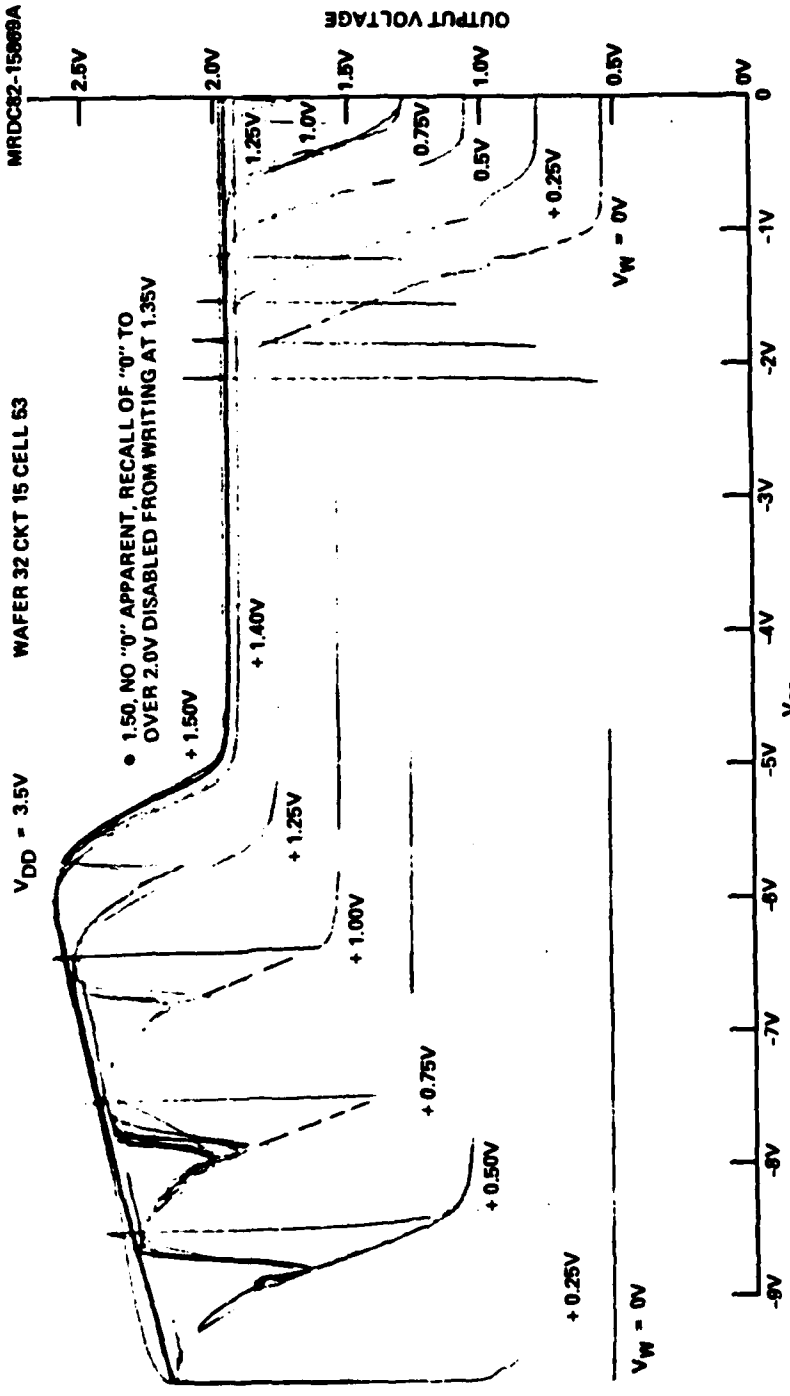


Fig. 3.3-5 Disabling characteristics of a RAM cell.

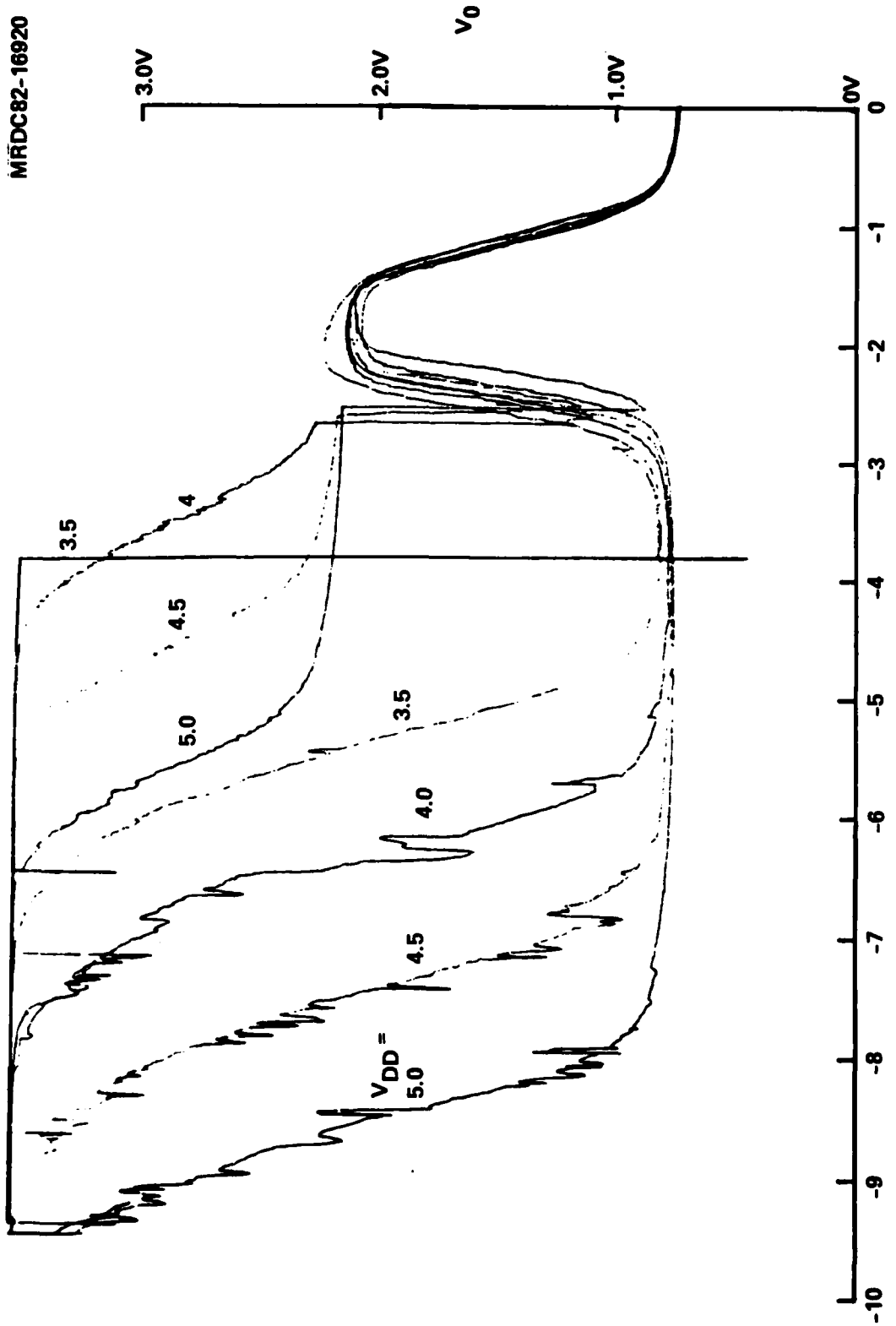


Fig. 3.3-6 Effect of V_{DD} variations on cell operation.

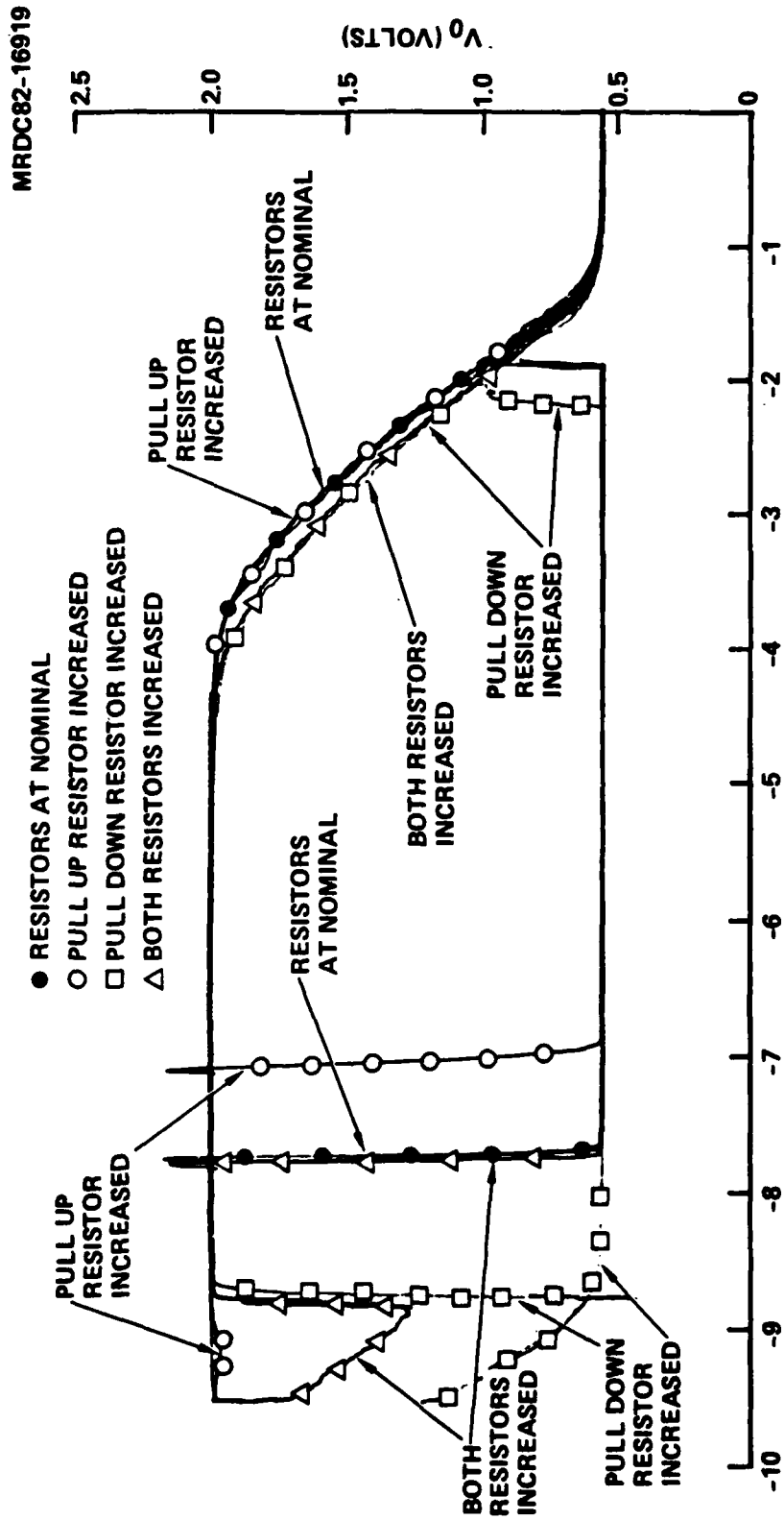


Fig. 3.3-7 Effect of 10% resistor variations on cell operation, measured on a cell with external resistors.

little effect. Increasing the pulldown resistor increased the window while increasing the pullup resistor decreased it, but not by large amounts. These data show that the cell design is not critically dependent on resistor values.

Some of the above data (e.g., resistor variation and word line voltage effects) were taken at lower values of V_{DD} (3.5 V or 2.5 V). There were two reasons for this: one is that the variation under study was more pronounced (i.e., caused a larger percentage variation with respect to V_{SS}) at lower values of V_{DD}, so testing at lower values of V_{DD} was done to aid analysis of circuit operation by accentuating the effect. The second reason was to cause the left hand portion of the operating window to occur at magnitudes of V_{SS} safely below the breakdown voltage of the circuit. All of the effects studied scaled to higher voltages without essential change, except a decrease in the percentage variation relative to V_{SS}.

Dynamic testing of the cell was also performed. As the word line voltage, V_W, is increased, the point is reached where a write pulse on the appropriate line does not change the state of the cell; the cell is then disabled. Disabling occurs for $V_W \approx 1.3$ V. As the word line voltage reaches 1.5 V, the output voltage is essentially the same for a stored "0" or a "1"; i.e., the operating loop traced out as V_{SS} is varied reduces to a line (or single curve). When V_W is again lowered the voltage is appropriate to the stored state, however. If V_W is raised high enough, then subsequently lowered, the output voltage will always be that for a "1", regardless of original state; the cell is "forgetting" data. The word line voltage, V_W for forgetting is greater than 2 V for all cells tested with $V_{DD} = 3.5$ V. For $V_{DD} = 5$ V, the forgetting voltage was $V_W \approx 2.4$-2.5 V.

One important parameter influencing memory cycle times is the minimum pulse width that can write, or change the state of, a cell. In dynamic testing, cells wrote "1" or "0" reliably and consistently with 2 ns pulses (the lower limit of the pulse generator). The cell design is therefore more than fast enough for a 10 ns access time RAM. In the course of the dynamic

testing, it became apparent that a larger output transistor is needed; tradeoff analysis of speed-to-load capability is still needed.

Preliminary yield testing was also completed on wafers from mask set AP1. Cells tested were the 2, 4 μm FET cells and the 3, 6 μm FET cells, both with tightened rules, and 1, 2 μm FET cells. The 2, 4 μm FET cells had a layout spacing error that caused a spacing in one location of 1 μm between Schottky metal lines instead of the usual 2 μm spacing. This error caused the yield of working cells to be ≈ 60%. Of interest was that every failed cell exhibited the same failure mode, and, when checked visually, showed a short due to this spacing error. Thus the spacing rule was verified, and otherwise high yield would be expected. The 3, 6 μm FET cell had a somewhat lower yield, and failures were not consistently due to a single cause. This result would be expected; the lower current densities in the FETs at these widths are well into the subthreshold region, and small parameter variations would have a greater effect on the cell operation than in the case of higher current density, smaller FETs. The 1, 2 μm cells showed fairly high yield. Analysis of the failure mechanisms for those cells is not complete, but the data are promising since smaller FETs (than 2, 4 μm) for which the increased current density will improve operation, may be viable from a processing standpoint.

4.0 PROGRESS ON 256 BIT RAM (RM2 MASK)

The AP1 mask fabrication and testing characterized the levels of diode voltage drop as a function of current, defined the maximum allowable pinch-off voltage for cell operation, and provided information on cell design and layout trade-offs relative to yield. These results provided a sound basis for the design, fabrication, and testing of a 256 bit RAM array.

4.1 RAM (256 bit) Design

The design approach taken for the second mask set, called RM2,* primarily focused on collecting yield statistics and was somewhat less concerned with achieving the 1.0 μW/bit power level. A notable change in the cell design of RM2 was to increase the current level in the diodes from 10 nA to 40 nA allowing cells with slightly higher pinch-off voltage FETs to be used. This change eased the design task of the decoder circuits that were to be included for the first time on this mask set. The baseline RAM cell for the 256 bit RM2 mask was designed for a 1.8 μW/bit power level; the layout is shown in Fig. 4.1-1.

Preliminary circuit designs were also made for the decoder circuit, shown in 4.1-2. These circuits, when tested, will provide data on the following: (1) the read current limiter and bit sense line charging and discharging characteristics; (2) cell disabling characteristics when driven by a gate output; (3) word line loading, and (4) verification of the power-enabling approach.

Arrays with variations on cell design, directed toward operation with higher pinch-off voltages, were also included. Three 256 bit arrays in all,

*The nomenclature of the two mask sets was derived as follows: the first was AP-x, from AOSP. When the mask was received, it was observed that it was difficult to distinguish between AP-x and AR-x used for masks on the DARPA program. Therefore the letter designation for the AOSP-RAM program was changed to RM-x from RAM-x.

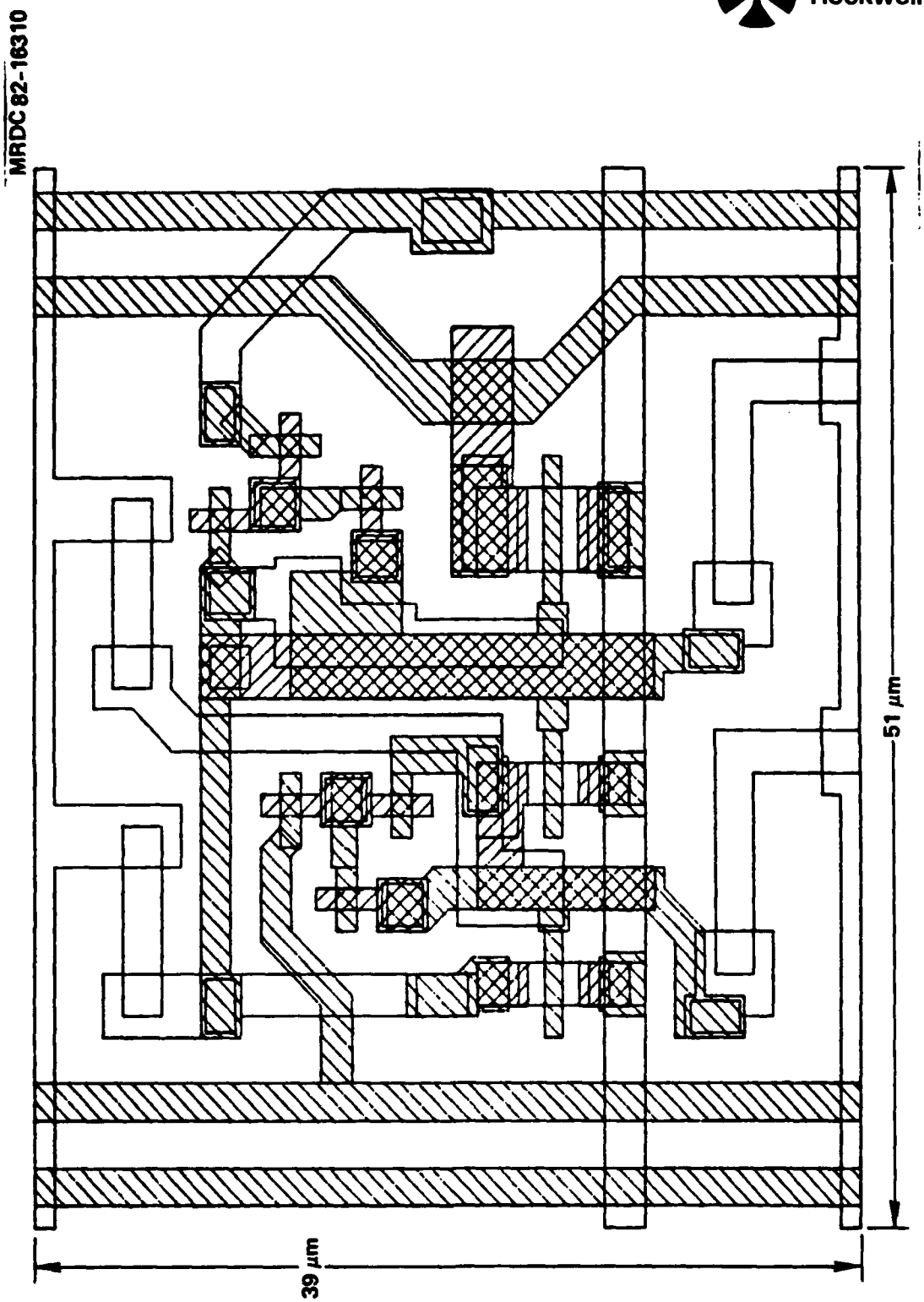


Fig. 4.1-1 GaAs static RAM cell.

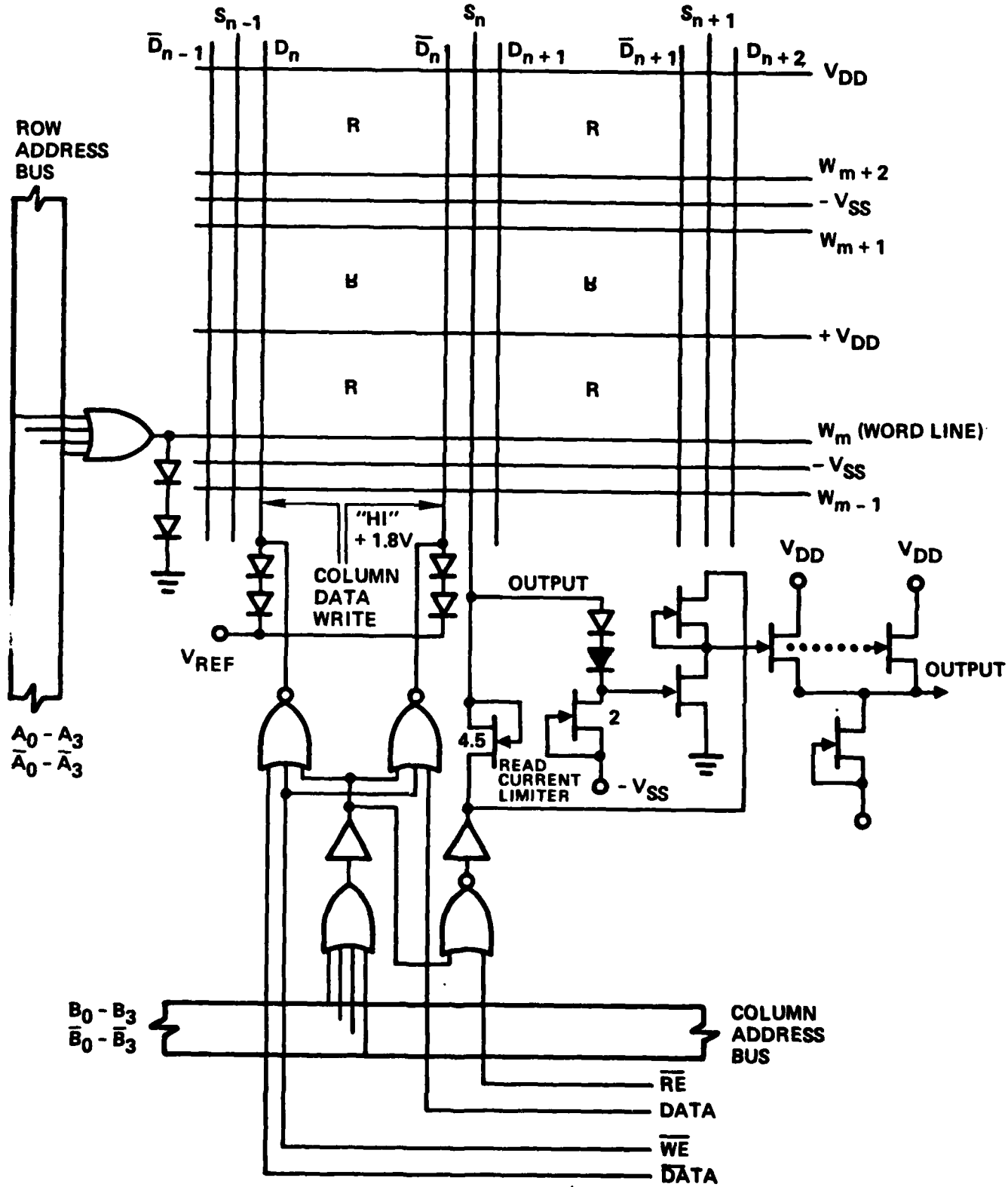


Fig. 4.1-2 Peripheral circuits for 256 bit static RAM (RM2).

with decoders, were included; these were, as shown in Table 4.1-1 (1) the baseline low power cell (40 nA in diodes), (2) a high power version with four times the current level (160 nA in diodes), and (3) a low current (40 nA in diodes) version with three diodes. Another array (with baseline cells) without decoders was also included for direct probing. Due to pad count and layout limitations, the size of this array actually was 14 × 16 = 224, rather than the full 16 × 16 = 256; the 224 size is sufficiently close to 256 that it virtually does not affect the yield study. The RM-2 mask organization is shown in Fig. 4.1-3, with the layout shown in Fig. 4.1-4.

Table 4.1-1

RM-2 Mask Set
Three Versions of RAM Cell

1. Low Power (Standard Version)

   - 22 and 50 megohm resistors
   - Power per cell: 2.3 μW enabled, 1.8 μW disabled

2. High Power (Will work with higher pinch-off voltages, but at higher power)

   - 6 and 12.5 megohm resistors
   - Power per cell: 8.4 μW enabled, 6.8 μW disabled

3. Three Diodes (Will work with higher pinch-off voltages while maintaining low power, but larger cell size)

   - 17 and 50 megohm resistors
   - Power per cell: 2.6 μW enabled, 2.0 μW disabled

4.2 RAM (224 bit) Testing

Testing of the undecoded arrays on RM-2 wafers was done, using an automated probe station and MACSYM Test computer. The test program exercises each cell in the RAM, reads the output and compares it against threshold, and

LOW POWER	3 DIODES LOW POWER	LOW POWER	3 DIODES LOW POWER	LOW POWER	3 DIODES LOW POWER
HIGH POWER	T2 | RES | CELL W/O RES NO PERIPHERALS LOW POWER	HIGH POWER	T2 | T1 | CELL W RES NO PERIPHERALS LOW POWER	HIGH POWER	T2 | RES | CELL W/O RES NO PERIPHERALS LOW POWER
LOW POWER	3 DIODES LOW POWER	LOW POWER	3 DIODES LOW POWER	LOW POWER	3 DIODES LOW POWER
HIGH POWER	T2 | T1 | CELL W RES NO PERIPHERALS LOW POWER	HIGH POWER	T2 | RES | CELL W/O RES NO PERIPHERALS LOW POWER	HIGH POWER	T2 | T1 | CELL W RES NO PERIPHERALS LOW POWER
LOW POWER	3 DIODES LOW POWER	LOW POWER	3 DIODES LOW POWER	LOW POWER	3 DIODES LOW POWER
HIGH POWER	T2 | RES | CELL W/O RES NO PERIPHERALS LOW POWER	HIGH POWER	T2 | T1 | CELL W RES NO PERIPHERALS LOW POWER	HIGH POWER	T2 | RES | CELL W/O RES NO PERIPHERALS LOW POWER

Fig. 4.1-3 256 bit GaAs RAM mask (RM2).

MRDC82-15868

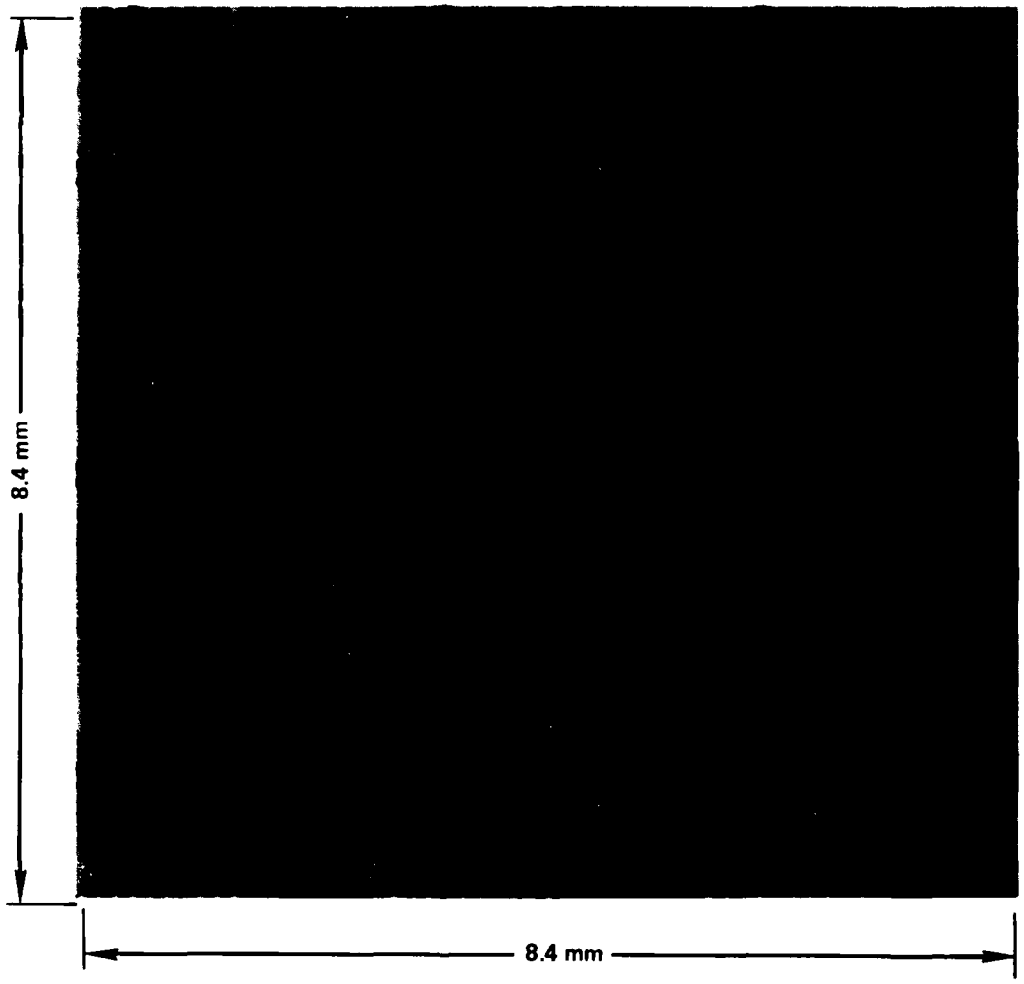


Fig. 4.1-4 256 bit GaAs RAM mask (RM2).

prints out errors. It also tests for storage of an initially written "1", after disabling and reenabling.

A special interface card provides the connections and terminations needed to connect the MACSYM to the probe card. Probes can also be connected to the column output lines for dynamic tests of one cell at a time, using an oscilloscope or an electrometer and recorder.

The test program goes through the following steps: it applies power to the circuit for testing; prints out current values and aborts the test if it finds a short; then cycles each cell in turn 5 times, writing alternately "0" and "1", leaving cells in the "1" state as it disables each row. After this cycling, each cell is addressed in turn. For each cell: (1) the output is read, digitized by comparing it to a reference, and an error flag set true or false; (2) a "0" is written, digitized, checked for error; and (3) a "1" is written, digitized and checked for error. The analog output voltages are stored in a matrix by row, column, and test condition (1, 2, or 3 above), as well as an error map (0 for no error, 1 for error) with the same matrix coordinates. While the test is in progress, any errors cause a printout (on the CRT) of address, test condition failed, and analog output voltage. At the conclusion of the test, a failure summary is printed out of the:

1. Number of cells failing to write a "0" or a "1",

2. Number of cells failing to write a "1",

3. Number of cells forgetting a "1" after being disabled,

4. Number of cells that failed both 2 and 3 above,

5. Total number of failures (both forgetting and failing to write).

A bit failure map can be printed out, as shown in Fig. 4.2-1. The top line gives date, wafer and chip number, and the failure summary per 1-5 above. The map, with row number on the left (to which 10 is added to make it two digit), displays 3 characters for each cell location, one for each of the three tests. ":--" implies all tests were passed; failure of any of the tests causes the number of that test to be printed in the corresponding location. The analog voltage for write "0" or write "1", along with row and column numbers, can also be printed out with the failure map. Figure 4.2-2 shows an example of a failure map with all three types of failures, and analog voltage printout. The last line of analog voltage printout, for example, shows the cell in row 5 (= 15-10), column 0 failed to write a "0", having an output voltage of 1.663 V (threshold was set at 1.60 V), while the third row shows the cell at row 1 (= 11-10), column 9 failed to write a "1", having an output voltage of 0.67 V.

These failure maps are being used as an aid, first, in visual inspection of failed cells to determine obvious failure causes, and then for subsequent, more thorough electrical testing. Data from this testing will be used to establish the yield model that will guide minor process, layout, and design modifications needed to attain the yield level required for producibility of 4K RAMs.

4.3 RAM (224 bit) Yield Analysis

The measurements made on the 224 bit arrays provide preliminary statistics on yield of the RM2 low power cell design. Four wafers were tested, each with 36 arrays of 224 bits per array. Thus 32,256 cells were available for test. Of the arrays, 3 had power supply shorts, and thus could not be tested. Therefore, 33 arrays (31,584 cells) were tested.

There were 14 perfect arrays, distributed 3, 3, 5 and 3 per wafer. The yield of perfect arrays was $14/(4 \times 36) = 10\%$. If Poisson statistics are assumed, the yield, Y, of an assemblage of n things, each having a probability of failure of p, is

```
03/10/62 11:27:02 RM2-11 15     NO. FAILED =0 0 1 0 1
10 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
11 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
12 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
13 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- 1--
14 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
15 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
16 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
17 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
18 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
19 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
20 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
21 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
22 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
23 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
24 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
25 :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :--
```

Fig. 4.2-1 Memory bit failure map.

```
)2/28/92 22:30:27 RM2-24 21      NO. FAILED =6 2 7B 2 82
:0 :-- 1-- 1-- 1-- 1-- 1-- :-- :-- :-- 1-- :-- :-- :-- 1--
.1 :-- :-- 1-- :-- :-- :-- 1-- :-- 1-- :-- 1-- :-- 1-- :--
.2 1-- :-- :-- :-- :-- :-- 1-- :-- 1-- :-- 1-- :-- :-- 1--
.3 :-- 1-- :-- :-- 1-- 1-- 1-- :-- 1-- :-- 1-- :-- :-- :--
.4 :-- :-- :-- :-- :-- :-- 1-- :-- 1-- 1-- :-- :-- 1-- :--
.5 :2- :-- 1-- :-- 1-- 1-- 1-- :-- :-- :-- :-- 1-- :-- 1--
.6 :-- :-- 1-- :-- :-- :-- :-- :-- :-- :-- :-- :-- 1-- :--
.7 :-- 1-- 1-- :-- 1-- :-- :-- :-- :-- :-- :-- 1-- 1-- 1--
.8 :-- 1-- :-- :-- :-- :-- 1-- :-- :-- :-- :-- :-- 1-- 1--
.9 :-- 1-- 1-- :-- 1-- 1-- :-- :-- :-- :-- :-- 1-- 1-- 1--
20 1-- :-- 1-- :-- :-- :-- 1-- :-- 1-- :-- :-- 1-- :-- 1--
21 1-- :-- :-- 1-- 1-3 1-- :-- :-- :-- 1-3 :-- :-- 1-- 1--
22 :2- 1-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- :-- 1--
23 :-- :-- :-- 1-- :-- :-- :-- :-- :-- :-- :-- :-- :-- 1--
24 :-- 1-- :-- 1-- :2- 1-- 1-- :-- 1-- :-- :-- :-- :-- 1--
25 :2- 1-- :-- 1-- :-- :-- :-- :-- 1-- :-- :-- :-- :-- :--
,J,K=  5        0        0        BJ =1.666
,J,K=  11       4        1        BJ =.651
,J,K=  11       9        1        BJ =.67
,J,K=  12       0        0        BJ =1.656
,J,K=  14       4        0        BJ =1.715
,J,K=  15       0        0        BJ =1.663
```

Fig. 4.2-2 Memory bit failure map with analog voltage printout.

$$Y = e^{pn} \quad .$$

Inversely,

$$p = \frac{-\ln Y}{n} = \frac{-\ln 0.1}{224}$$

$$P = 1.02\%$$

or the implied probability of failure of a cell, at least for this set of good arrays, is around 1%.

The failure rate over the arrays tested is as follows:

1. The total of all cells tested was 31,584; the total number of cells that were observed (by the computer) as working was 29,094. The ratio of these numbers is an upper bound on the failure rate. This upper bound on failure rate is 7.9%.

2. Many of the failures were of a row or column (either whole or partial). Such failures obviously are more probably due to a single failure (a broken metal line or something similar) that affects the other cells. Such a failure should be called only one failure, since the other cells probably work if they could be accessed. When this kind of pattern recognition approach is used to infer the most probable rate, counting all arrays, the failure rate is 1.9%.

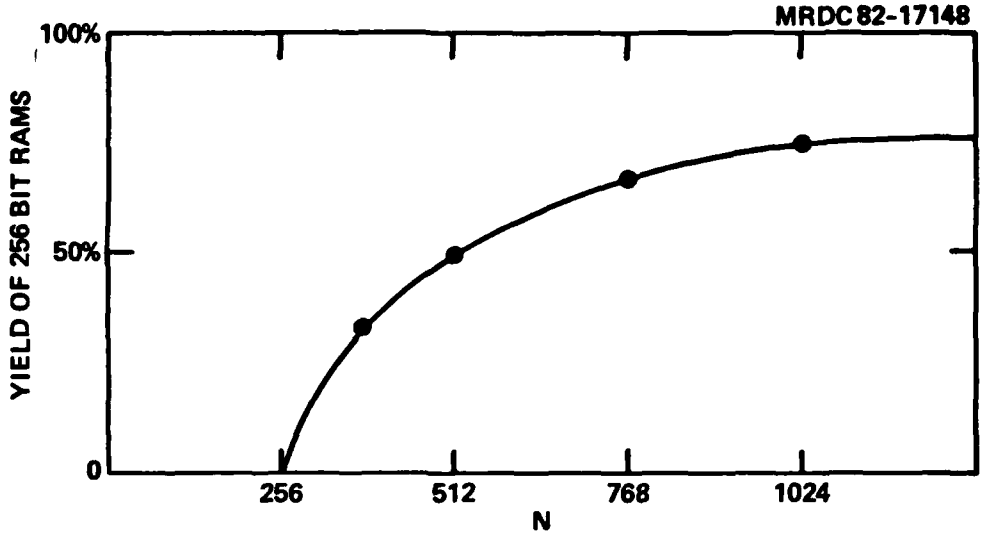
3. Some arrays had a number of cell failures much higher than the wafer average or that of adjacent arrays. It is as though a larger area defect occurred. Such arrays should be culled, and not counted in the statistics. If these arrays (of which there

were 17) are deleted from the statistics, for the remaining better arrays the inferred most probable failure rate is ≈ 1.0%. This compares closely with the value inferred from perfect arrays. Therefore, individual cell yield is estimated to be of the order of 99% for the four wafers tested.

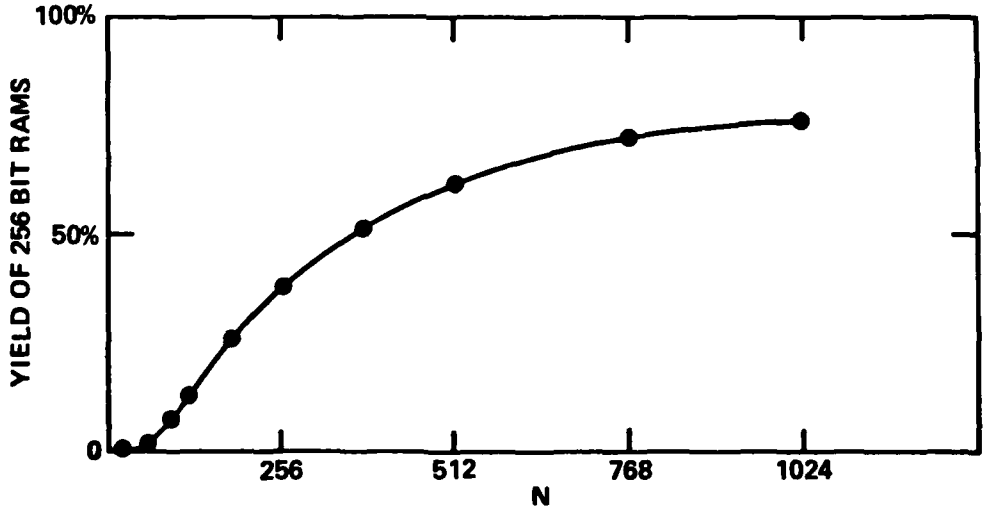
Alternatively stated, the failure rate, for these four wafers, is one in 100.

The meaning of the yield for a 4K design can be assessed by considering how cell failure rate affects potential yield. A good intuitive feel for the problem can be gained as follows: visualize a continuous, infinitely long row of cells. Conceptually, the task of fabricating a 256 bit (or 4K) RAM is the same as taking consecutive 256 bit (or 4K) segments from that row. The reciprocal of the failure rate is the average number of good cells in the row between failed ones. If it is assumed for the moment that the average number of good cells between successive failed ones is the actual number for all cases (i.e., that the average itself has a zero standard deviation), the yield calculation is simple; in Fig. 4.3-1a a plot is shown of yield of 256 bit RAMs, according to this simplified model. If the failure rate is one in N, for N less than 256 the yield of 256 bit RAMs will be zero. For N = 257, the yield will be small but non zero; as N doubles to 512, the yield will be 50%. The main point is that the yield increases rapidly for N > 256 (or failure probability < 1/256 ≈ 0.4%).

If the assumption of a fixed number of good cells (0 standard deviation of average number of good cells) is removed, the number of good cells will be random, with a Poisson distribution. The effect of this randomizing is shown in Fig. 4.3-1b. Compared to the previous example, the yield for a one in 256 failure rate is now 37%, and for one in 512 is 60%. The significant effect of the randomizing is to increase the yield for N approximately equal to, but also considerably less than, the size of RAM being considered. The real case with the RAM should be close to the randomized case. The variation of yield with failure rate for a 4K RAM is shown in



a) FAILURE RATE = ONE IN N



b) FAILURE RATE = ONE IN N

Fig. 4.3-1 Yield of 224 bit RAMs as a function of reciprocal failure rate for: (a) simplified non-statistical model, (b) randomized Poisson model.

Fig. 4.3-2. The implication of cell yield statistics on the design of a 4K RAM is now clear. Yield of a 4K RAM will be achieved, not by refining the design of a 4K part, but by refining the design -- including circuit design, layout, and processing -- of the cells, in any size array, to achieve a failure rate of the order of one in 2000-4000. For a failure rate of one in 1000, the anticipated yield of 4K RAMs is approximately 2%, which can be considered a threshold of viability. Any further decrease in failure rate increases yield to a practical range. The failure rate obtained with the present design (one in 100) must therefore be decreased by a factor greater than 10; a (4K RAM) factor of 20 decrease would result in a yield of 13%.

The yield currently achieved, for essentially a first design, is an adequate starting point to lead to a 4K RAM design. The steps needed are to continue testing, and to do very thorough failure analysis to categorize the failure mechanisms. Designing out the failure mechanisms that occur most frequently will result in a new design with a lower failure rate.

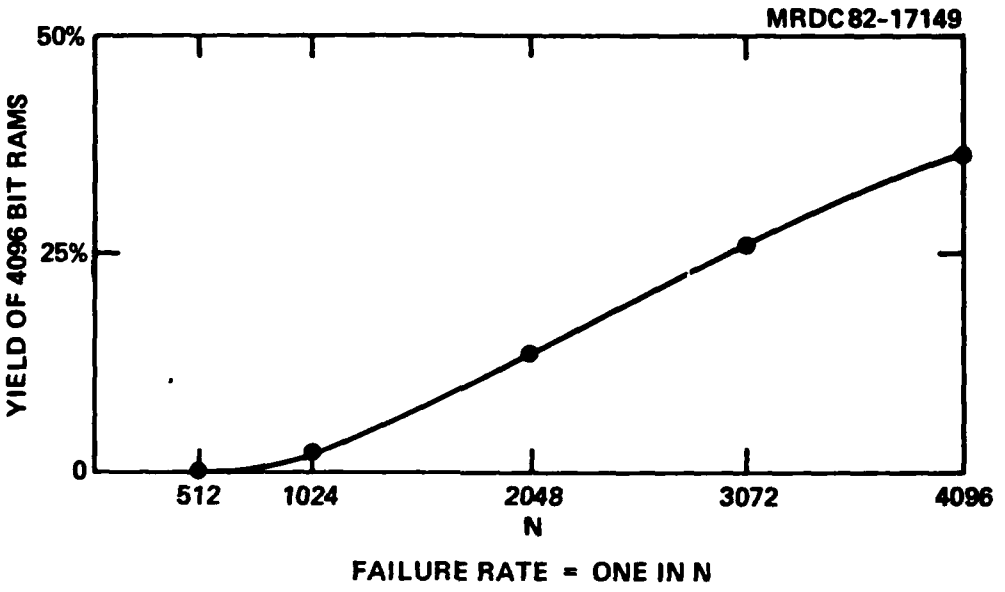


Fig. 4.3-2 Yield of 4K RAMs as a function of reciprocal failure rate.

5.0 RADIATION TESTING

Total dose radiation experiments were carried out using one of the wafers from the first mask set, AP1-11. This wafer was irradiated with a total gamma dose of 10^7 rad and the following parameters were measured before and after irradiation: (1) the substrate leakage current, (2) the subthreshold conduction of the FETs, and (3) the I-V characteristics of the diodes. With the exception of a slight change in diode forward voltage drop, no change in characteristics occurred due to radiation exposure. Test results from wafer AP1-11 are described in detail below:

Substrate Leakage Current - The substrate leakage current was evaluated by measuring the I-V characteristics of the isolation test pattern. This pattern was 50 μm wide with a 3 μm gap between the two n^+ implants. The negligible decrease in substrate current, as shown in Fig. 5.1, demonstrates that the isolation properties of the GaAs substrates are unaltered by irradiation.

Subthreshold Characteristics - The subthreshold characteristics of a small FET (gate dimensions 24 μm wide by 1 μm long) before and after irradiation are shown in Fig. 5.2. The slight shift in the log I vs V_{gs} curve represents a decrease in the magnitude of the effective threshold voltage of approximately 15 mV. It is noteworthy that the slope of the curves in the low current region does not change. Gate leakage current was less than the measurement sensitivity during both tests. The conclusion is that 10^7 rads caused no significant change in FET subthreshold characteristics, the slight actual change observed being in a direction to improve circuit operation.

Schottky Diode Characteristics - The Schottky diode characteristics before and after irradiation are shown in Fig. 5.3. The ideal

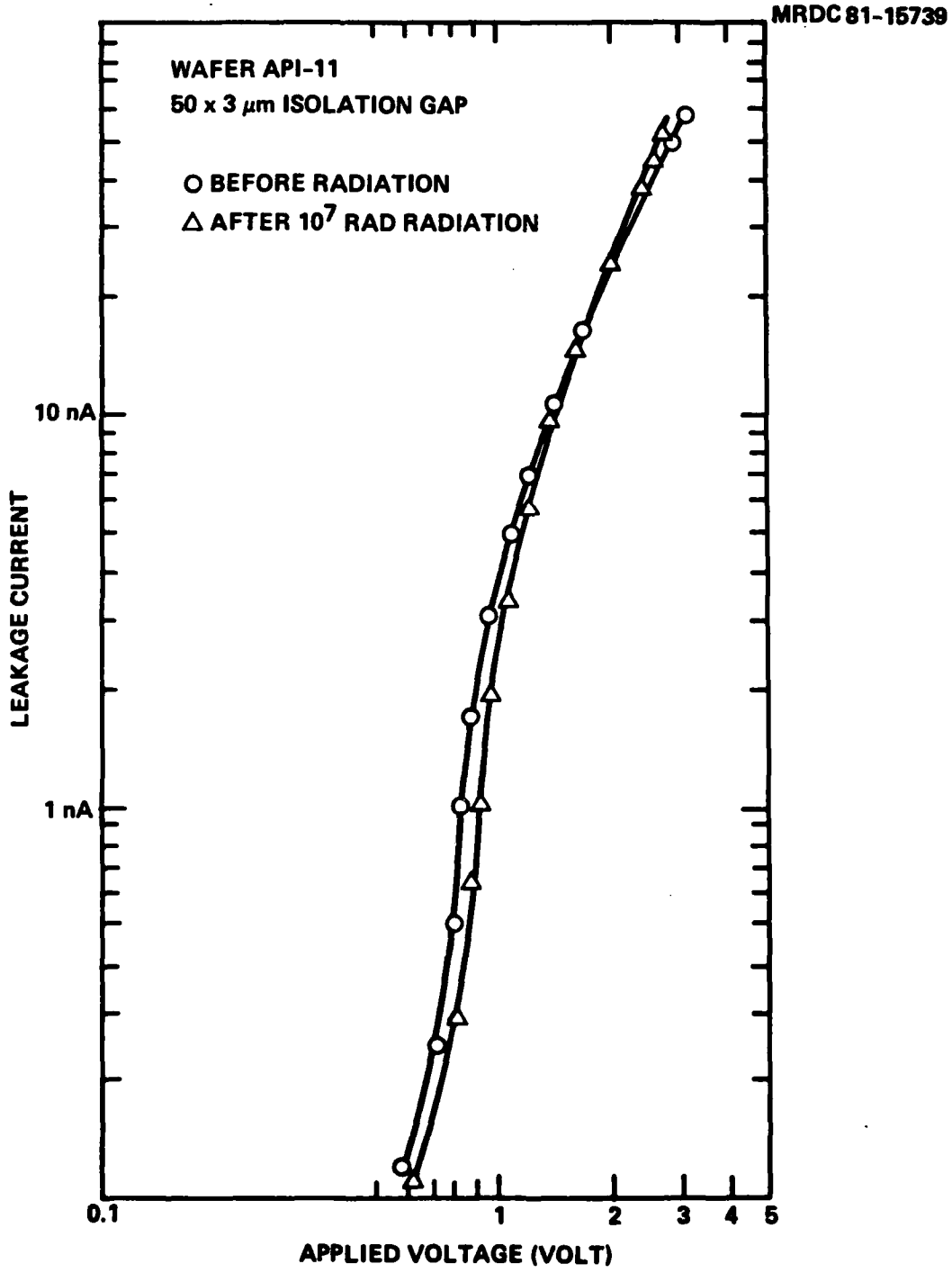


Fig. 5.1 Substrate leakage measurements.

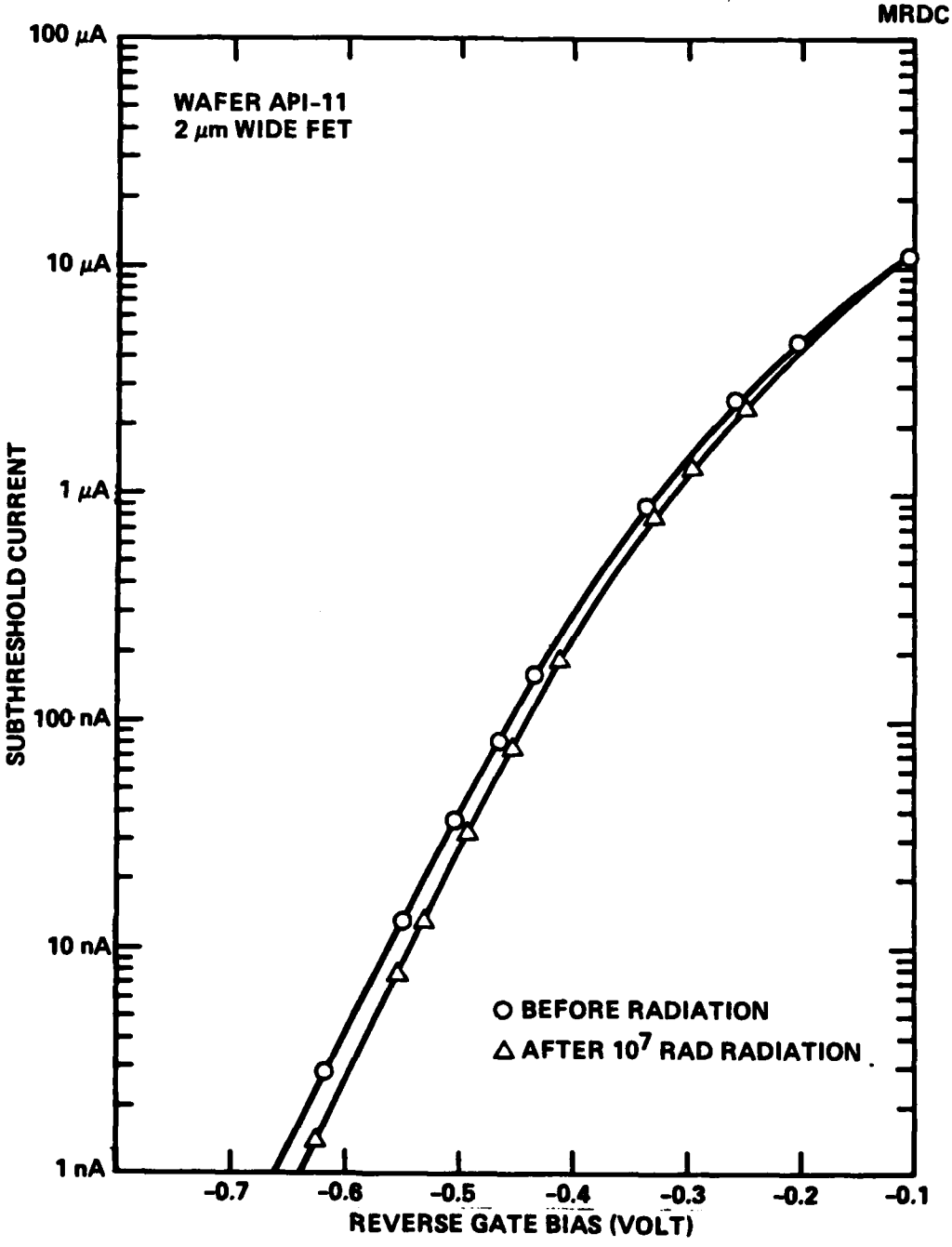


Fig. 5.2 Variation of subthreshold current with radiation.

MRDC82-15781

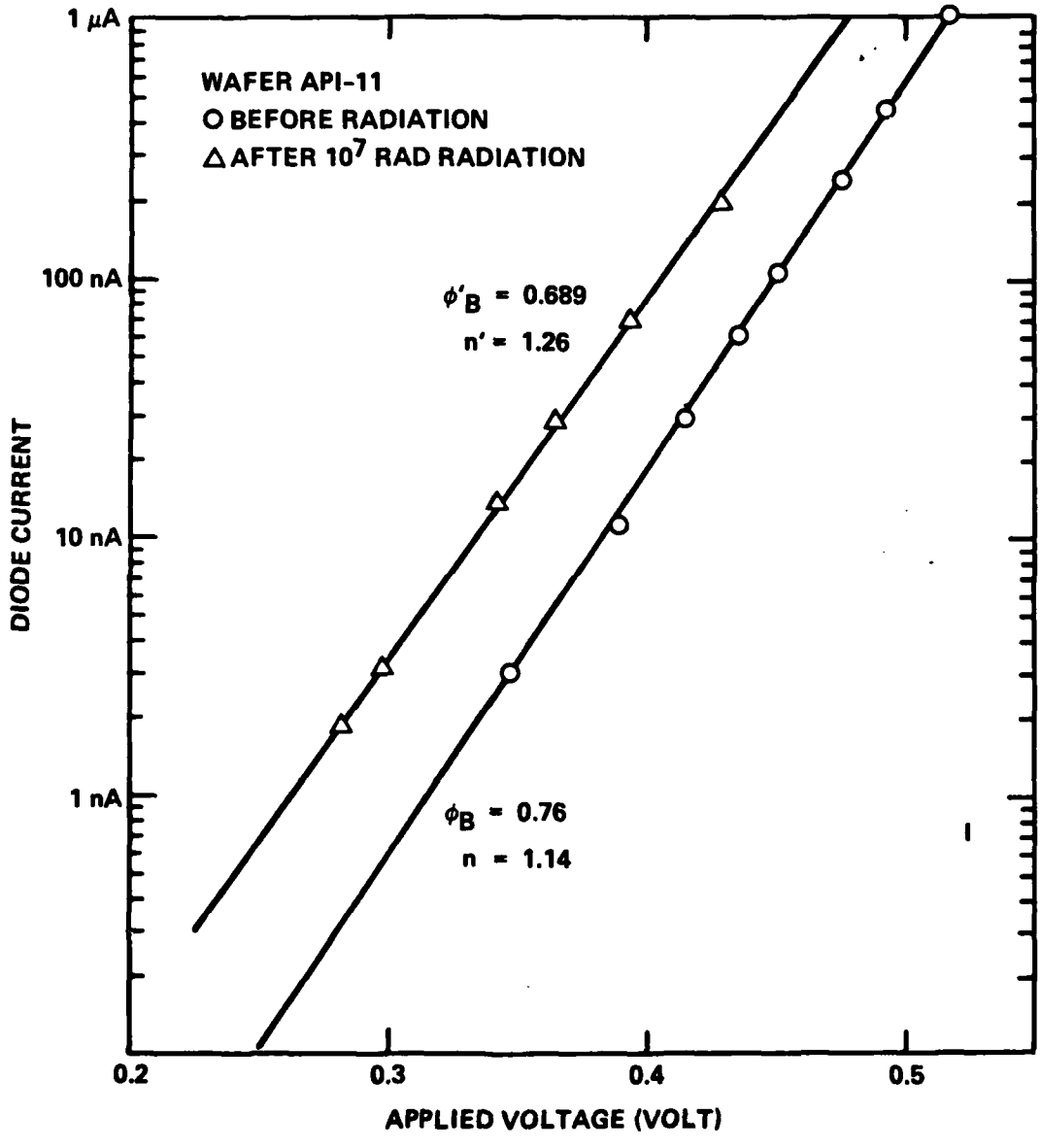


Fig. 5.3 Diode characteristics before and after radiation.

characteristic of the Schottky junction remains unchanged after irradiation, as indicated by the linear relation of the log I vs V curve. The most notable change is a decrease in barrier height of approximatly 70 mV, as well as a small increase in the ideality factor n. The lower barrier height causes an upward shift in the log I vs V curve, and therefore a reduction in the forward voltage drop across the diode at a given current. The magnitude of the change is approximately 50 mV for currents in the tens of nanoamperes. In the case of the RAM cell, the decrease in forward voltage tightens the design restrictions, but it should be partly compensated by the accompanying slight decrease in FET threshold voltage. These preliminary test results are indicative of the small magnitude of radiation effects. The small voltage shift occurring in the diodes can be accounted for in the design of the circuit, and therefore should not be a problem.

A number of other device parameters, such as FET threshold-voltage, saturation current, and K value also show a slight but unimportant change after irradiation of 10^7 rads. Table 5.1 shows the average value and the standard deviation for these parameters both before and after irradiation. The slight decrease in the saturation current, I_{DSS}, after irradiation is not expected to effect the operation of the RAM cell which operates at current levels much lower than I_{DSS}. A fully functional RAM cell was also tested dynamically before and after irradiation; oscillograms of multifunction operation are shown in Fig. 5.4 (a) and (b). The data output shows writing "1", writing "0", and remembering both "0" and "1" when re-enabled after being disabled. The same voltages were applied in both cases. The absence of any apparent change indicates that cell operation is insensitive to the slight shift in the characteristics of the devices caused by irradiation of 10^7 rads.

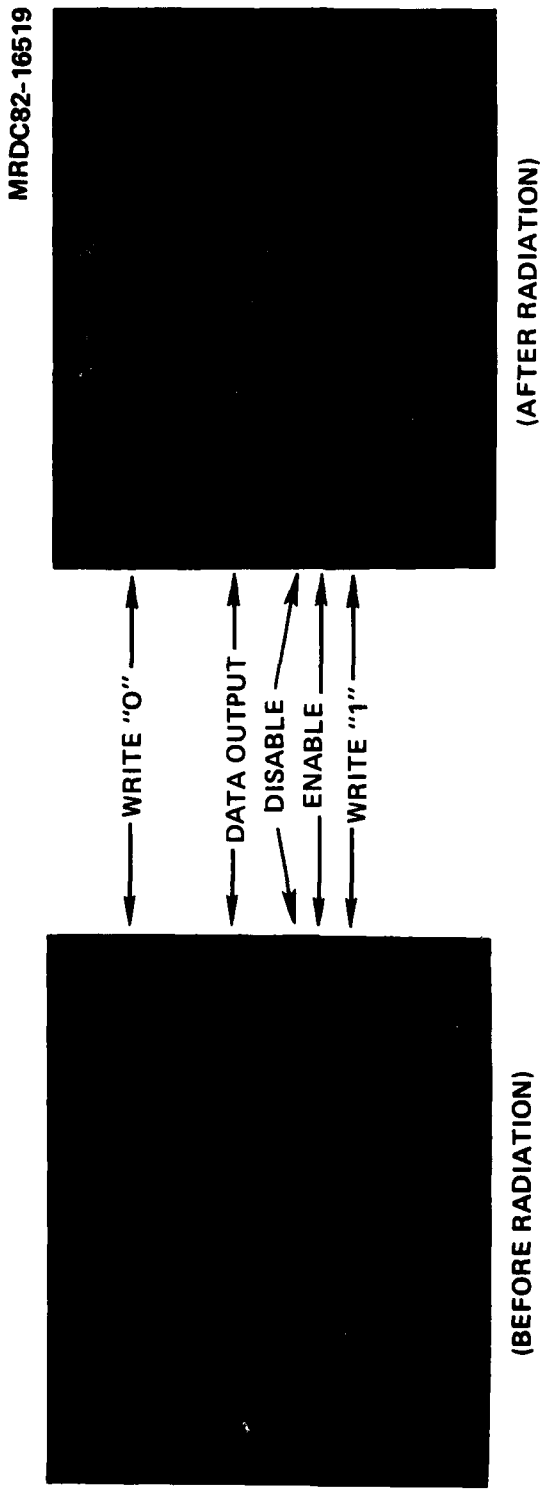


Fig. 5.4 Fully functional RAM cell after total dose radiation of 10^7 rad.

Table 5.1

50 μm × 1 μm Gate FET

Variation in Threshold Voltage, Saturation Current, and K Value Before and After 10^7 Rads. The Following Data is the Average of 35 FETs

	$-V_P$ (volts)	σ_{V_P} (volts)	I_{DSS}	$\sigma_{I_{DSS}}$	K (ma/V^2)	σ_K (ma/V^2)
Before Radiation	0.493	0.100	0.800	0.264	3.395	0.366
Before Radiation	0.504	0.100	0.787	0.258	3.149	0.300

6.0 REFERENCES

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2. C.P. Lee, S.J. Lee and B.M. Welch, "Carrier Injection and Backgating Effect in GaAs MESFETs," IEEE Electron Device Letters, April 1982.